Bus Interface Products

1991 Data Book

Advanced
Micro
Devices

Am29C800A

Advanced Micro Devices

Bus Interface Products

1991 Databook

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Increasing integration and performance in today's state-of-the-art systems requires corresponding improvements in bus interface. AMD's Am29C800A Family meets this challenge, offering the system designer a variety of 9 and 10-bit wide interface solutions with the speed and drive characteristics of bipolar products and the low power consumption of CMOS. We are confident you will find these devices suitable for your most demanding applications.

Fred J. Roeder
Vice President
Standard Products Division

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NUMERICAL DEVICE INDEX

Introduction

This handbook contains applications information, qualification data and product specifications for the Am29C800A CMOS High-Performance Bus Interface Family as well as a section on the bipolar Am29800 devices available. The bipolar and CMOS families provide wide (9-bit and 10-bit) data-path solutions in a variety of functions for use in various performance sensitive system applications.

The Am29C800A High-Performance CMOS Bus Interface Family provides bipolar-comparable speed and drive performance while consuming much less power. Pin-for-pin compatible with the Am29800 bipolar device families, the Am29C800A Family has the same functionality, features, and performance with 48 mA output drive. The Am29C800A devices offer lower propagation delays and consume less power than their bipolar and CMOS predecessors. Manufactured with AMD's advanced CS-11SA process technology, the fast switching speeds and low noise requirements for today's high speed systems are achieved.

EASIER SYSTEM DESIGN
At AMD, we think realistic propagation delay performance that makes designing your system easier is more useful than unrealistic specs that look good on paper. That's why our new Am29C800A Bus Interface Family has the fastest usable speed of any high performance CMOS bus interface family.

CONTROLLED EDGE RATE OUTPUTS IMPROVE RELIABILITY
Our proprietary output circuitry significantly reduces the effects of simultaneous switching noise (ground bounce), undershoots, and overshoots which can cause bus contention, data loss, and system crashes. Controlled-edge rates slow down high-to-low output transitions (3–4 ns typical) and cut-off diodes reduce voltage transients. For more detail see the included application note "Minimization of Ground Bounce Through Output Edge-Rate Control."

TTL COMPATIBLE OUTPUTS
The Am29C800A proprietary output structure also includes n-channel pull-up transistors which reduce output voltage transitions to TTL levels. This results in far less noise generation than standard CMOS outputs.

GLITCH-FREE POWER UP/DOWN
All Am29C800A products have proprietary power up/down circuitry which disables the outputs during power cycling. This facilitates the design of card-edge applications which often require power down for card replacement.

48 mA DRIVE
All Am29C800A products (except the Am29C818A) supply 48 mA output drive which is required by many of today's standard and proprietary system buses. This drive capability is also useful for interfacing with buses that have heavy capacitive loads and run at high bus frequencies.

LOW POWER CMOS
The Am29C800A Bus Interface Family is produced with the same state-of-the-art submicron process technology as AMD's 29K™ RISC microprocessor. This technology provides the dual benefits of low power consumption with the superior noise immunity of CMOS.

SOLUTIONS FOR REAL WORLD PROBLEMS

AMD's Bus Interface Family makes designing fast PC's, workstations, fileservers, peripherals and other performance-driven systems easier by providing the ground bounce and voltage swing protection required in addition to fast usable speed.

PACKAGING

The family is available in a variety of popular packages, including 24-Pin Slim (300-mil) Plastic DIP, 24-Pin Small Outline (SOIC), and 28-Pin Plastic Leaded Chip Carrier (PLCC) for commercial devices. Military versions are available in 24-Pin Slim (300-mil) ceramic DIP packaging.

CHAPTER 2
General Product Information

General Product Information

DEVICE TESTING INFORMATION

Test Philosophy and Methods

The following paragraphs give the general philosophy that is applied to tests that must be properly engineered if they are to be implemented in an automated test environment. The specifics of what philosophies are applied to which test are shown in the data sheets and the data sheet reconciliations that follow.

Capacitive Loading for AC Testing

Automatic Test Equipment (ATE) and its associated hardware has stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that require smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float-delays" that measure the propagation delays into the high-impedence state, and are usually specified at a load capacitance of 5 pF. In these cases, the ATE test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench set-up are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical ATE is not capable of switching loads in mid test, it is impractical to make measurements at both capacitances, even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench set-up and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data sheet loads, may be used for production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of devices near threshold frequency give rise to oscillations when testing high-speed circuits. These circuits are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" HIGH and LOW levels are used for other tests. Generally, this means that function and AC testing are performed at "hard" input levels.

AC Testing

Some AC parameters cannot be measured accurately on automatic testers because of tester limitations. In these cases, the parameter in question is tested by correlating the tester data to bench data.

Certain AC tests are guaranteed by correlating to other tests that have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

When performing I_{SC} tests on devices containing latches or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements, which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{OUT}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result is identical to the $V_{OUT} = 0$, $V_{CC} = $ Max. case.

Switching Test Circuit for Am29C800A/Am29800A (Except for Am29818A)
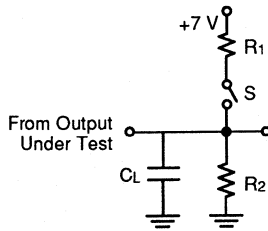
11128-012A

Three-State Outputs

Switch Positions For Parameter Testing

Parameter	S Position
t_{PLH}	Closed
t_{PHL}	Closed
t_{HZ}	Open
t_{ZH}	Open
t_{LZ}	Closed
t_{ZL}	Closed

Switching Test Circuit for Am29818A
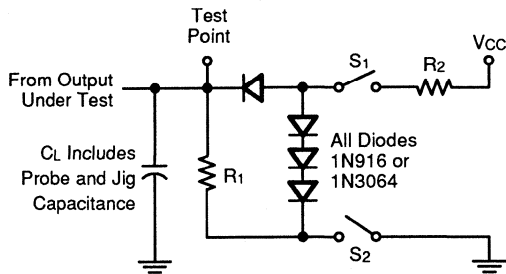
11128-013A

Pin	R_1	R_2
$Y_0 - Y_7$	1K	280
D_{0-7}	5K	2K

Three-State Outputs

Switching Test Circuit for Am29818A (Continued)
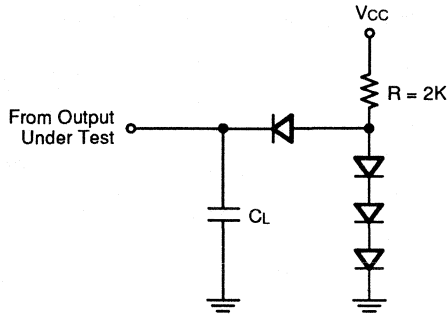
11128-014A

SDO Output

Switching Test Circuit for Am29800
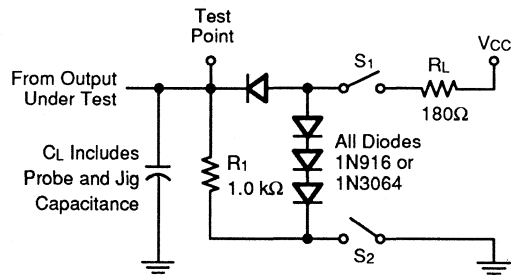
11128-015A

Load Test Circuit

Switching Test Waveforms
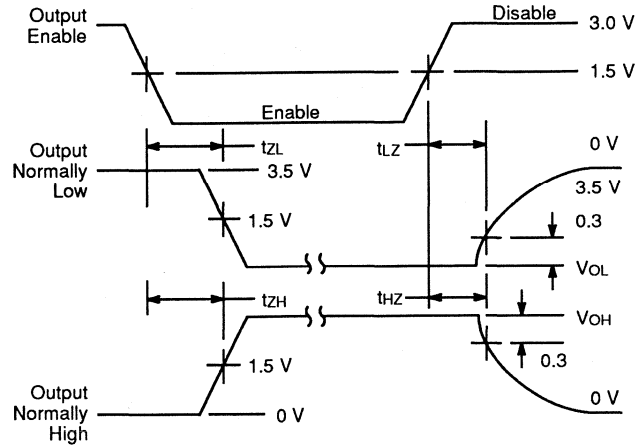
11128-016A

Enable and Disable Times
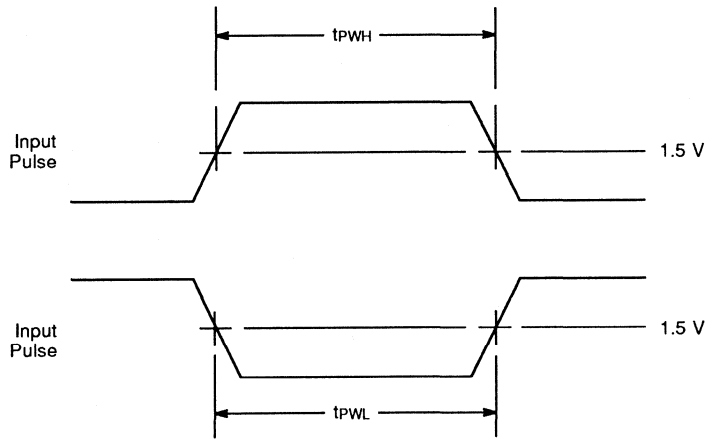
11128-017A

Pulse Width
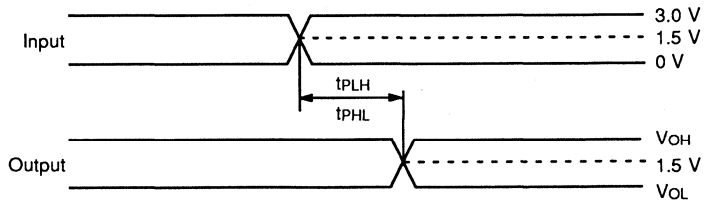
11128-018A

Propagation Delay for Buffers, Transceivers, and Latches in the Transparent Mode

Switching Test Waveforms (Continued)
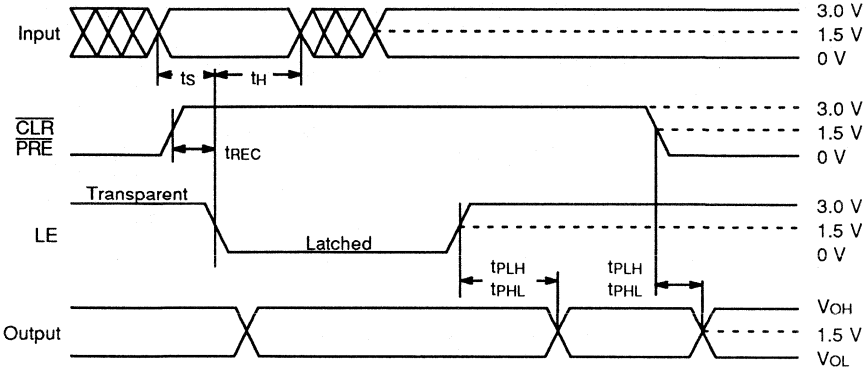
11128-019A

Switching Parameters for Circuits with Latches
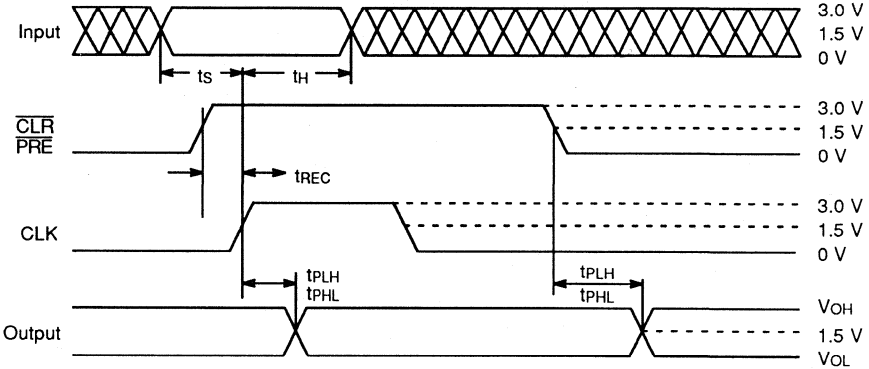
11128-020A

Switching Parameters for Circuits with Registers

Am29C800A QUALIFICATION INFORMATION

The following qualification information summary has been included to aid the user with component evaluation and production release.

Device Process/Die Information

1) Process Name: CS11SA
2) Process Technology: CMOS
3) Wafer Fabrication: Fab 15, Austin, Texas
4) Die Size:

> 84 x 129 mils for Am29C821/23A/27A/28A/41A/43A
> 117 x 124 mils for Am29C833A/53A/61A/63A

5) Internal Die Revision: "D"
6) Bond Pad Size: 125 x 125 μm
7) Substrate: N$^-$epi over N$^+$, P$^-$ well
8) Gate Oxide Thickness: 200 Å
9) Number of Metal Layers: 2
10) Metal Thickness: 0.32 μm/1.0 μm
11) Content of Metalization:

> 1st level – Ti/TiN-0.5%Cu/Al-MoSi
> 2nd level – Al

12) Minimum Metal Line/Spacing Width:

> Metal 1 – 2.4 μm width, 1.44 μm spacing
> Metal 2 – 4.16 μm width, 1.76 μm spacing

13) Contact Dimensions (via's):

> Contact 1 – 1.28 μm x 1.28 μm
> Contact 2 – 1.60 μm x 1.60 μm

14) Passivation Material: 4% LTO/Nitride
15) Passivation Thickness: 7000 Å/8500 Å
16) ESD Protection: > 2000 V

Assembly/Package Information

1) Assembly location: Malaysia, Philippines, and Korea
2) Test location: Malaysia or Sunnyvale, California

For PDip/SOIC Packages

3) Resin Indentification: Epoxy Novolac
4) Package Compound: Sumitomo 6300H
5) Filler Content: Fused Silica
6) Thermal Conductivity: >13 x 10^{-4} calorie/cm. °C.sec
7) Glass Transition Temperature: 155°C
8) Die Attach Material: Silver Filled Epoxy
9) Die Attach Material Vendor: Dexter Hysol
10) Wire Bond Metal: 1.25 mil gold wire
11) Wire Bond Method: Thermosonic
12) Lead Frame Material: Copper
13) Lead Frame Finish: Solder Dip (PDip), Solder Plate (SOIC)

For Ceramic/Cerdip Packages

14) Sealing Process: Dry air seal furnace
15) Body Material: 90% Al_2O_3
16) Lid Material: 90% Al_2O_3
17) Die Attach Material: Silver Glass
18) Die Attach Material Vendor: Johnson Mathey Incorporate
19) Wire Bond Metal: Al
20) Wire Bond Method: Ultrasonic Wedge Bonding
21) Lead Frame Material: Alloy 42
22) Lead Frame Finish: Solder Dip

TYPICAL PERFORMANCE DATA

To help system design-in activities, we are providing the following typical information. This data represents production material for the Am29C800A family, but is not guaranteed.

Am29C800A Typical Capacitance Values

The following table shows typical zero bias capacitance values for plastic packages.

Output to GND	Output to Vcc	Input to GND	Input to Vcc
15 pF	15 pF	15 pF	15 pF

Typical Switching Speeds vs. Load Capacitance

AC delays in the Am29C800A data sheets are specified for 50 pF and 300 pF output loads. In most cases, parameters specified at 50 pF load are production tested, whereas parameters specified at 300 pF are guaranteed by characterization data, but not tested in production. Figure 2–1 shows the typical effects of increased capacitive loads on propagation delays. Note that this graph displays typical derating, over the entire Vcc and temperature range.

Am29C800A Typical Switching Speeds vs. Load Capacitance
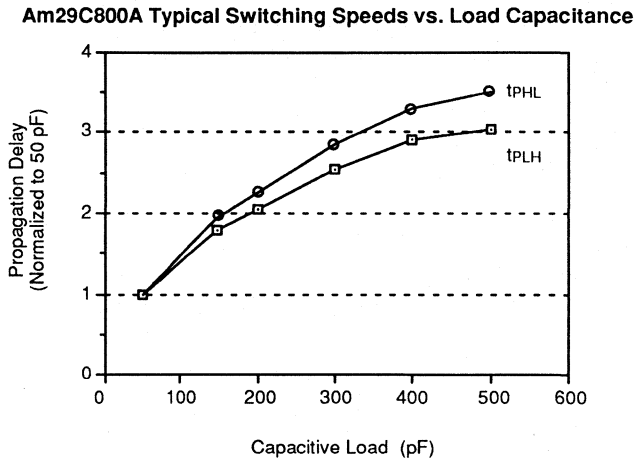
11128-001A

Figure 2–1

Typical Switching Speeds vs. Number Of Outputs Switching for Am29C800A

Some degradation of propagation delay is normally experienced when several outputs switch simultaneously. By industry convention, data sheet limits are specified for only one output switching. To assist the system designer, the following graphs show typical speed degradation in the Am29C800A Family (see Figures 2–2 & 2–3).

Typical Switching Speeds vs. Number of Outputs Switching
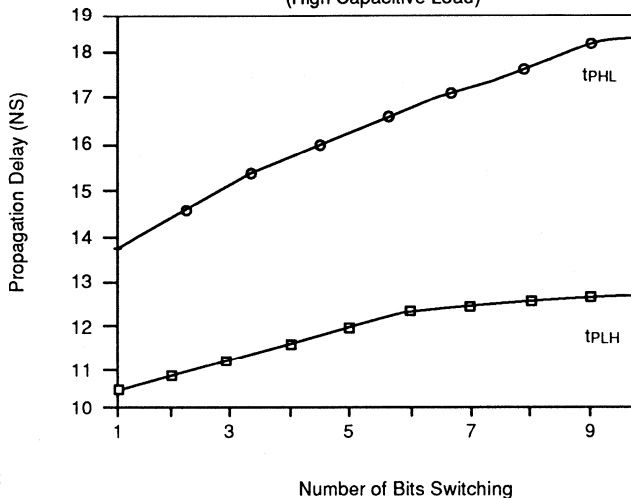
11128-002A

Note:

470 pF @ 25°C.

Figure 2–2

Typical Switching Speeds vs. Number of Outputs Switching
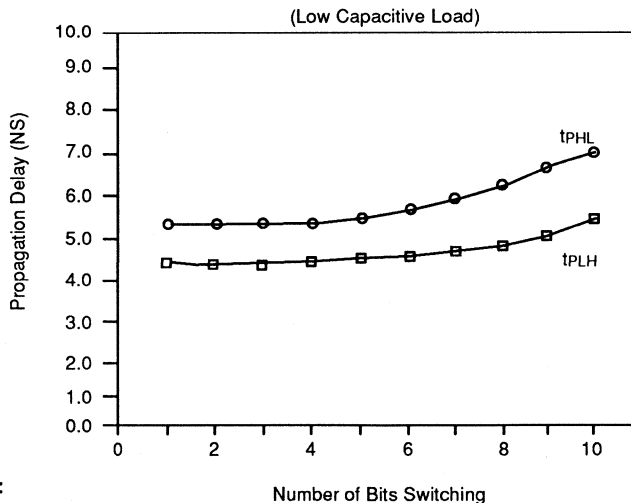
11128-003A

Note:

50 pF @ 25°C.

Figure 2–3

Note that the graphs on page 2–10 are to be used as design guidelines and should not be used to generate specification limits.

The measurements for deriving this graph were taken on a carefully built AC jig in a noise-free environment. All outputs were loaded according to data sheet specifications, and in the case of buffers and transceivers, all inputs were switched simultaneously from the same signal source.

It is important to note that conditions external to the device can also contribute to speed degradation. For example, inductance of PC board traces, inefficient GROUND and Vcc planes, and inadequate bypassing can cause significant GROUND and Vcc bounce which will in turn degrade AC delay when several bits are switched simultaneously. In the case of buffers and transceivers, input signal skew will cause a sustained disturbance of internal threshold due to a protracted GROUND bounce within the device. This can result in further degradation of AC delays. These conditions are application-specific. Therefore, if a system designer sees speed degradation much in excess of the guidelines given, a closer look should be taken at board layout and the application.

ESD Protection
All Am29C800A devices are protected from ESD damage up to 2000 V.

Simultaneous Switching Considerations (The "Ground Bounce Phenomenon")
High current drive, short propagation delays, and fast logic level transitions at the output are the characteristics of TTL-compatible high-speed bus interface circuits, such as those in the Am29C800A and Am29800 family of products. When they are used in high-performance systems, simultaneous switching of several outputs is a common occurence. During such switching, noise is generated due to rapid changes in the drive currents (di/dt) and their interaction with the parasitic inductance (L) of the bonding wires and package leads associated with the Vcc, GROUND and output terminals. This section describes the nature of this noise, its impact on circuit behavior, and the measurements that can be taken by the IC vendor and the system designer to minimize the effects of this noise.

Description of the Problem
The problem is best described with reference to a simplified first-order equivalent circuit of the output of a high-speed bus interface device. Switches S1 and S2 represent active pull-up and pull-down structures. L1, L2, and L3 represent the parasitic lumped inductances associated with the Vcc, GROUND and output terminals of the device (see Figure 2–4). The output switches are designed to carry high currents so that fast TTL logic level transitions can occur at the output in the presence of heavy capacitive loading.
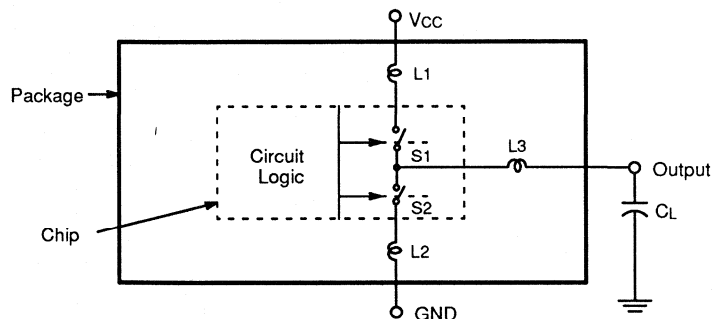
11128-004A

Figure 2–4. Equivalent Circuit of Bus Interface Output

During the switching of an output, rapid changes occur in the current levels in the V_{CC}, GROUND, and output leads due to the load charging current and the "overlap" current through switches S1 and S2 if these switches turn on simultaneously for a short time. The resulting di/dt and its interaction with L1 and L2 disturb the static voltage levels at the device V_{CC} and GROUND pads. This superimposed noise at the internal power supply nodes is commonly referred to as the "V_{CC} and GROUND BOUNCE." Since the magnitude of this noise is a function of di/dt, it is higher when several outputs switch simultaneously.

As an example, consider a 24-lead ceramic DIP package with a GND pin (pin #12) inductance of 15 nH. A di/dt of 50 mA/ns caused by simultaneous switching of multiple outputs will result in a GROUND bounce of 15 x 50 = 750 mV magnitude. Note that parasitic effects external to the package are ignored in this calculation.

Effects of Ground and V_{CC} Bounce

The total magnitude of the V_{CC} and GROUND noise caused by di/dt and parasitic inductances is a function of circuit configuration, package characteristics, and PC board layout external to the device. Depending on the magnitude of the bounce, one or more of the following effects may occur in a system environment:

1. When several outputs are switching simultaneously, the static logic level of an unswitched output may be disturbed, and may cross the input logic recognition level (V_{IH} or V_{IL}) of the circuits connected to that output.
2. Non-monotonic transitions may occur at the switched outputs due to violation of noise immunity within the circuit.
3. Circuits with storage elements, such as latches and flip-flops, may experience loss of data due to false clocking or latching of erroneous data.
4. A protracted disturbance of voltage levels at internal nodes may cause significant degradation of propagation delays when several outputs are switched simultaneously.

System Design Considerations

The following guidelines will help the system designer minimize the adverse effects of V_{CC} and GROUND bounce when using high-speed interface devices in a high-performance system.

1. GROUND and V_{CC} planes must be used to minimize parasitic effects. Wire-wrap boards will exacerbate the noise problem.
2. Use of sockets or device carriers must be avoided since these will add to the parasitic inductance and increase power supply noise.
3. It is recommended that each device be bypassed directly at the power pins with a high-frequency bypass capacitor in addition to the normal bypassing scheme.
4. Simultaneous switching of several control lines coincident with the switching of multiple outputs should be avoided.
5. Use of a package type that has lower pin parasitics will help minimize the effects of power supply and ground noise. AMD offers surface mount devices (in PLCC, LCC, and SO) which reduce the lead inductance associated with the V_{CC} and GND pins.
6. If possible, system timing can be adjusted to allow for setting time before reading the data on the bus.
7. External series damping resistors can be used on the outputs that are subjected to simultaneous switching. This will slow down the transition times and reduce di/dt effects.
8. By reducing the loading on the circuits that drive sensitive control lines such as CLOCK, CLEAR, PRESET, and LATCH ENABLE, noise immunity can be improved at these inputs.

Summary

Package lead inductance and other parasitics contribute to the noise induced in high-speed, high-drive integrated circuits. This noise gets worse if multiple outputs are switched simultaneously and can cause performance degradation. The system designer should be aware of the problems associated with high-speed switching and should carefully evaluate the application and system considerations.

Am29C800A Typical Ground Bounce Information

In a system environment, noise induced on the "quiet output," due to the simultaneous switching of all the other active outputs, becomes very critical. Therefore to help the system engineer designing his/her system, we have included two photographs of typical Ground Bounce behavior for Pdip package using our Am29C800A device. However, one should note that ground bounce measurements may vary significantly due to set up differences. The test conditions for both photographs are done at V_{CC} = 5 V, 5.5 V, T_A = 25°C and load = 50 pF/500 Ω. The first 'bounce' in each photograph represents the change on ground line when all the other outputs are switching from Low to High, and the second 'bounce' represents the change when the other outputs are going from High to Low.

T_A = 25°C
V_{CC} = 5.00 V
Photo 1.
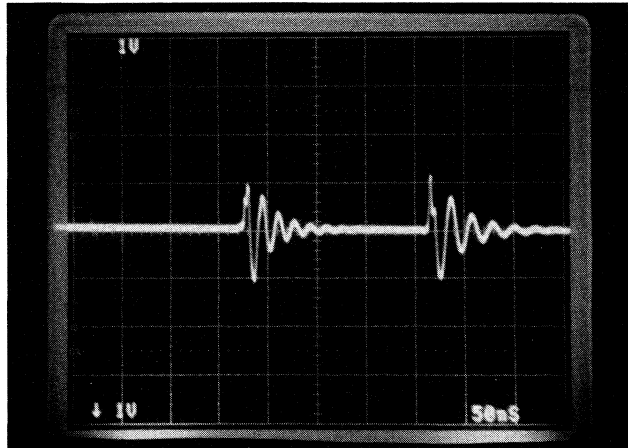
T_A = 25°C
V_{CC} = 5.50 V
Photo 2.
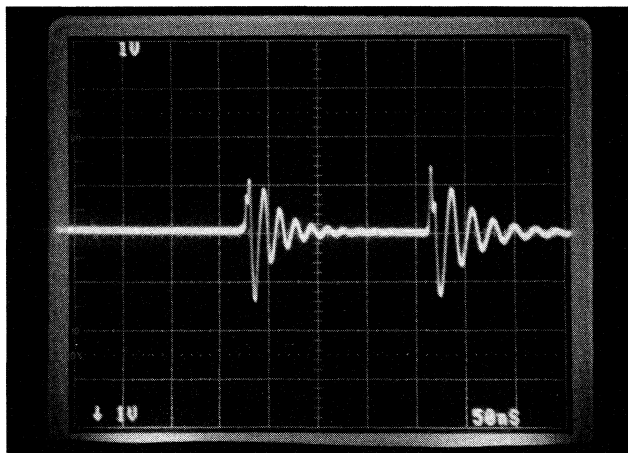
Note:
Vertical Scale: 1V/div
Horizontal Scale: 50 ns/div

POWER DISSIPATION CONSIDERATIONS FOR CMOS DEVICES

Introduction

CMOS bus interface devices (8, 9, and 10 bits wide) are rapidly invading the arena previously dominated by bipolar devices. This is because CMOS technology has made sufficient progress to provide an alternative to bipolar in terms of both high-speed and high-drive. In addition, at low data rates, CMOS devices offer much lower power dissipation when compared with their bipolar counterparts. However, there are some overzealous claims made with regard to this "power advantage." Statements such as "stingy CMOS consumes negligible power when driving high-speed buses" are to general and can be misleading. This report explains the basics of switching in CMOS circuits and provides guidelines for calculating power dissipation in CMOS parallel interface circuits.

Definition of Terms

$I_{CC(Q)}$ — Quiescent power supply current

$I_{CC(T)}$ — Power supply current component per input at TTL HIGH level

$I_{CC(D)}$ — Dynamic power supply current expressed in $\mu A/MHz/bit$

f — Equivalent toggle frequency at the output

C_L — Load capacitance per output

C_i — Lumped equivalent circuit capacitance per bit

Power Supply Current Components

A CMOS circuit operating in a TTL environment has three power supply current (I_{CC}) components. The total I_{CC}, when multiplied by V_{CC}, will determine the total power dissipated in the device.

The first component is the quiescent current $I_{CC(Q)}$. This is the leakage current through the device when all inputs are tied to either V_{CC} rail or GND, and all outputs are open (no load). This current is typically in the microamps region, and represents STAND-BY (or quiescent) power dissipation, its contribution to the total power dissipation is insignificant at high data rates.

The second component is $I_{CC(T)}$, the current in TTL-compatible input stages. Because of the difference in threshold for N-channel and P-channel devices, each input stages offers a DC path from V_{CC} to GND. This I_{CC} component is a function of input voltage applied. Figure 2 shows a typical $I_{CC(T)}$ characteristic as a function of V_{IN}.
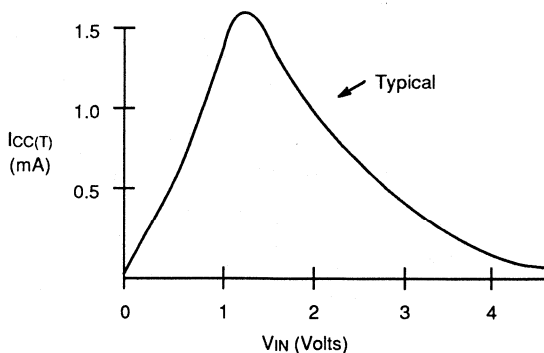
11128-005A

Figure 2–5. Typical $I_{CC(T)}$ as a Function of V_{IN}

Considering "realistic" worst-cast conditions, $I_{CC(T)}$ is normally specified at $V_{IN} = 3.4$ V. Its value is given on a per input basis. To determined the total $I_{CC(T)}$ per device, one needs to know the number of inputs and the duty cycle for those inputs in HIGH state.

Note that the $I_{CC(T)}$ component applies to CMOS circuits operating in a TTL environment and driven by bipolar TTL circuits. In an all-CMOS environment, the driving signals (input signals) to such interface circuits will be close to V_{CC} rail or GND. In such cases $I_{CC(T)}$ is not applicable.

The third component is the dynamic power supply current – $I_{CC(D)}$. This current represents the power dissipated in the device in order to charge and discharge internal node capacitances in the device as well as any external load connected to the outputs. This component is a function of operating frequency and load capacitance, and dominates the total I_{CC} at high data rates. Therefore it is discussed in further detail in the following sections.

Back to Basics

Consider a simple buffer gate. Figure 2–6 shows the lumped equivalent capacitance of the circuit internal to the device. This capacitance C_i is charged rail-to-rail at frequency f. When the gate has load C_L at the output as shown in Figure 2–7, this load is also charged rail-to-rail.
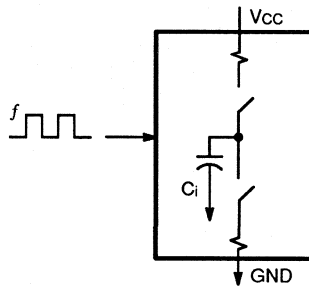
11128-006A

Figure 2–6. Unload Buffer
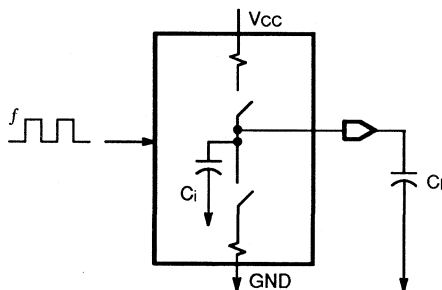
11128-007A

Figure 2–7. Buffer with Load C_L

Basic theory leads us to the equation $P = f \, CV_{CC}^2$ where P is the dynamic power dissipation in the gate. Since $P = IV_{CC}$ where I is the average current in the V_{CC} line, we get:

$$I = f \, CV_{CC} \quad -------- (1)$$

Equation (1) shows that there is a linear relationship between I and frequency. By obtaining values of I for different values of f, one can derive a normalized expression for current I per MHz. For the unloaded case, this equation is:

$$I_{CC(D)} = C_i \, V_{CC} \; \mu A/MHz/bit \quad ----- (2)$$

where V_{CC} is in volts and C_i is in pF. Equation (2) enables us to obtain the value of C_i per bit if $I_{CC(D)} = 200$ mA/MHz/bit at a given V_{CC}. For example, if $I_{CC(D)} = 200 \; \mu A/MHz/bit$ at $V_{CC} = 5 \, V$, then:

$$C_i = 200/5 = 40 \text{ pF/bit}$$

If the output has a load C_L, it is effectively added to C_i, and $I_{CC(D)}$ will be higher as a result (see equation 2). If C_i is estimated, $I_{CC(D)}$ for a loaded case can be computed by using the formula:

$$I_{CC(D)} \, @ \, C_L = I_{CC(D)} \; \frac{C_L + C_i}{C_i}$$

For the example just given,

$$I_{CC(D)} \, @ \, 50 \text{ pF} = 200 \; \frac{50 + 40}{40} = 450 \; \mu A/MHz/bit$$

$$I_{CC(D)} \, @ \, 300 \text{ pF} = 200 \; \frac{300 + 40}{40} = 1.7 \text{ mA/MHz/bit}$$

To get a good feel for the numbers, consider a 10-bit buffer, with 300-pF load on each output, running at an "average" 5 MHz rate. The dynamic I_{CC} component will be:

$$I_{CC(D)} = 10 \text{ bits x } 1.7 \text{ mA/bit x 5 MHz} = 85 \text{ mA}$$

The term "average" rate used in the example above needs some explanation. Since the dynamic I_{CC} is attributed to a signal transitions, its value is highest when all outputs have a 1010... pattern at the data rate. However, such a pattern on a continuous basis is not realistic because it does not contain any information, except, of course, in a clock driver application. Therefore, to obtain a "realistic" worst-case $I_{CC(D)}$, one needs to estimate an average reate based on expected number of transitions. This average rate is lower than the data rate.

Total Power Supply Current (An Example)

For any given condition, the total Icc is given by:

$$Icc \text{ (total)} = Icc_{(Q)} + Icc_{(T)} + Icc_{(D)}$$

Consider the following specification for the 10-bit buffer used in the last example:

Icc(Q)		= 150 μA
Icc(T)	– Data Inputs	= 1.5 mA/input @ 3.4 V
	– Control Inputs	= 3.0 mA/input @ 3.4 V
Icc(D)	– Unloaded	= 0.2 mA/MHz/bit

To find the total Icc at a data rate of 10 MHz (50% duty cycle) when all outputs have 50-pF load:

1. Icc(Q) = 0.15 mA

2. Icc(T) = 10 bits x 1.5 mA per bit x 0.5 = 7.5 mA*

* Control inputs (such as $\overline{OE}$) are assumed to be at logic LOW; therefore their contribution to Icc(T) is ignored.

3. $Icc_{(D)}$ @ 50 pF = $0.2 \dfrac{50 + 40}{40}$ = 0.45 mA/MHz

<div align="center">(see example shown earlier)</div>

Therefore:

Icc(D) for the device = 10 bits x 0.45 per bit x 10 MHz = 45 mA

Total Icc = 0.15 + 7.5 + 45 = 52.65 mA

Summary

A system designer needs to consider all components of power supply current, and calculate the total Icc based on the frequency of operation and loading. This is particularly important if CMOS parallel interface devices are used in high-speed bus applications.

Am29C800A Typical I_{CC(D)} vs. Frequency Plots

For CMOS devices, I_{CC} is very dependent upon the frequency of operation. The next four graphs (Figures 2–8, 2–9, 2–10, 2–11) show the increase in dynamic I_{CC} as frequency increases. These graphs represent typical performance over the V_{CC} and temperature operating ranges and are not included in production testing. The load used for the measurements is 50 pF/500 Ω.
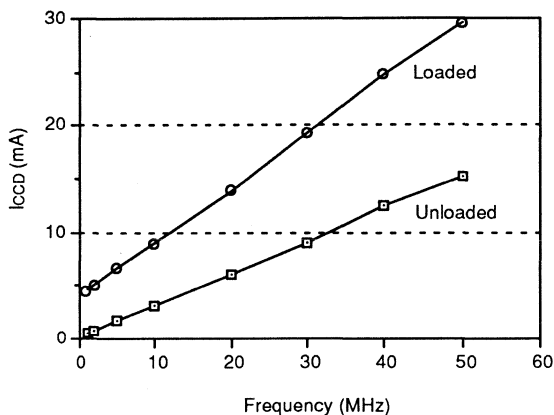
11128-008A

Figure 2–8. Registers (Am29C821A/23A)
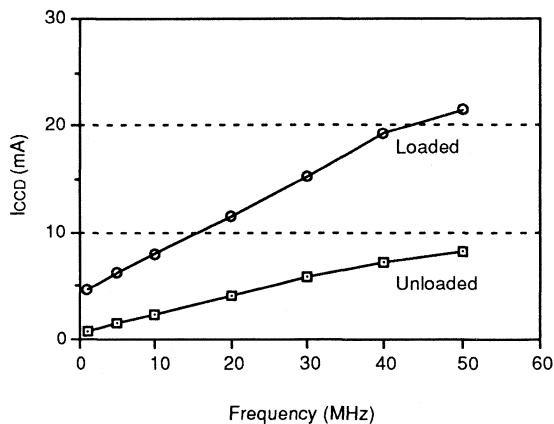
11128-009A

Figure 2–9. Buffers (Am29C827A/28A)
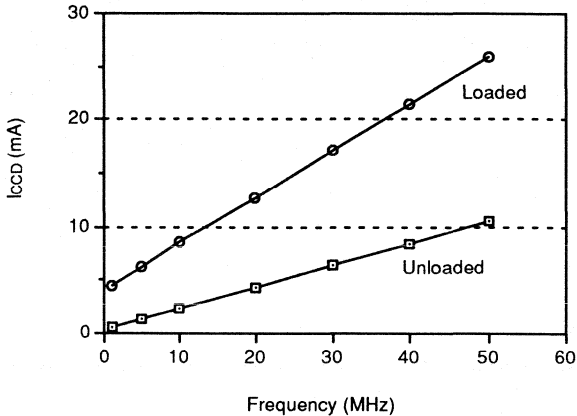
11128-010A

Figure 2–10. Latches (Am29C841A/43A)
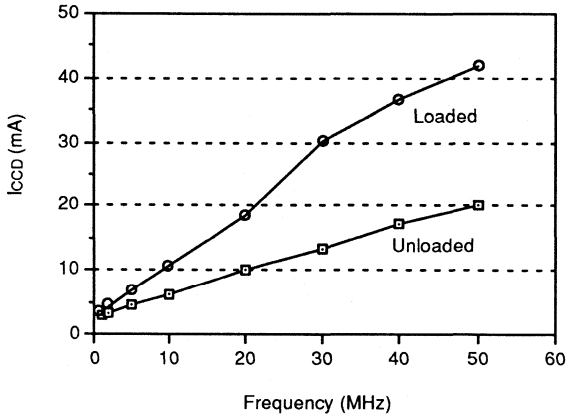
11128-011A

Figure 2–11. Transceivers (Am29C833A/53A/61A/63A)

DEVICE GATE COUNTS/THERMAL CHARACTERISTICS
Device Gate Counts

Part Number	Equivalent Number of Gates
CMOS	
29C818A	303
29C821A	90
29C823A	96
29C827A	60
29C828A	55
29C833A	139
29C841A	73
29C843A	69
29C853A	135
29C861A	105
29C863A	98
Bipolar	
29818A	147
29821	72
29823	68
29825	61
29827	11
29827A	30
29828	11
29833A	88
29841	52
29843	49
29853A	84
29861	22
29863	20

Thermal Characteristics

	Parameter	SOIC	PDIP	Unit
CMOS	θ_{JA}	85	67	°C/W
	θ_{JC}	11	10	°C/W
BIPOLAR	θ_{JA}	79	63	°C/W
	θ_{JC}	11	10	°C/W

CHAPTER 3
Minimization of Ground Bounce Through Output Edge-rate Control

Minimization of Ground Bounce Through Output Edge-Rate Control

By: Bernie New

The development of fast, high-current integrated circuits has brought about a phenomenon known as ground bounce. This is especially noticeable in bus-driving applications, where individual devices can have multiple outputs switching very high currents simultaneously.

There are three symptoms associated with the phenomenon:

- Outputs switching from HIGH-to-LOW exhibit excessive ringing, which may cause multiple transitions at inputs connected to that output.

- The ringing also appears at non-switching outputs which are in the LOW state. This may also cause unwanted transitions at inputs connected to those outputs.

- If the device contains storage elements, the ringing may corrupt the data stored in these elements.

Ground bounce is associated with parasitic inductance and resistance in the power-supply connections. These parasitic effects exist within all integrated circuits and may not totally be eliminated. Poor board design will also contribute to the problem. The following discussion covers the cause of ground bounce in CMOS circuits, and describes AMD's output-driver circuit design that minimizes the problem. Accompanying photographs show an example of the driver in operation.

THE IDEAL DRIVER

Figure 1 shows an ideal totem-pole output driver. The two transistors are switched on alternately, the upper one for a logic '1', and the lower one for a logic '0'. Apart from a brief period of overlap during switching, the two transistors are never on together. For the high-impedance state of 3-state outputs, both transistors are turned off. The load connected to the totem-pole output is adequately modeled as a parallel R-C circuit.
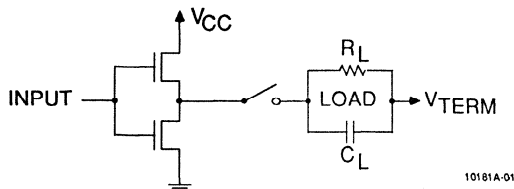
Figure 1. Ideal Driver

While this is an ideal driver, it is not constructed with ideal transistors. Each transistor has a finite impedance when in the 'on' state. This impedance manifests itself in three ways; it affects the slew rate of the output, the dc level of the output, and it limits the short-circuit current.

Before a transition, the load capacitor is charged according to the current output state ('0' or '1'). When the output transistors switch, they charge or discharge the load capacitor, and their impedance is part of the R-C time constant, which determines the slew rate of the output. In this respect, lower impedance is better. With a lower impedance, the load capacitance can be charged or discharged to the required output level faster, thus permitting higher operating speeds.

When the output voltage has stabilized at the desired logic level, the dc current flowing through the transistor impedance creates a residual voltage across the transistor (I-R drop). The output voltage specifications require that this residual voltage be kept below maximum values (V_{OL}). Again, a lower impedance is better, allowing higher output currents at any given V_{OL}.

However, even in the ideal case, the impedances should not be arbitrarily small, since they also control short-circuit current. If an output is inadvertently connected to one of the power supplies, or to a second output in a different state, these impedances will limit the power dissipation in the device and prevent potential destruction.

It would appear that the optimum design would be to make the impedance just large enough to protect the device under short-circuit conditions, while maximizing slew-rate and drive capability. This assumes that die area is not a consideration, since low impedance transistors are physically large. However, in the real world, parasitic effects cause this choice to lead to far from optimum results.

THE REAL WORLD

The practical problems that arise concern parasitic effects in the connections to the transistors. Between the output of the driver and the load, there is a small bond wire and a trace from the package bonding pad to the external pin. These connections are both resistive and inductive.

A similar parasitic impedance is also found in the ground pin of the device. Additionally, it is not possible to locate all outputs physically close to the ground connection on the die. The deposited metal trace that connects the output driver to the ground pad also contributes parasitic resistance and inductance.

In the circuit of Figure 2, only effects in the ground connections are shown. Similar parasitics must exist in the V_{CC} connections but, since requirements for V_{OH} are less demanding, higher-impedance pull-up transistors can be used. This reduces the effect of the parasitic impedance. Experience has shown the problem to be associated with the HIGH-to-LOW transition and outputs in the LOW state, hence the name ground bounce.

Before a HIGH-to-LOW transition, the load capacitor is charged to the HIGH state. During the transition, the pull-up transistor turns 'off' and the pull-down transistor turns 'on' to discharge the load capacitor. The very low impedance of the pull-down transistor causes the parasitic impedances to interact with the load to form a step-excited L-C-R network. This results in ringing on the output.

While the output might quickly reach V_{OL}, it will not remain there due to the ringing. The output may not be considered a LOW until the output has stabilized to the point that it remains below V_{OL}. During the ringing, the output could exceed the actual threshold (as opposed to V_{IH}, the guaranteed input HIGH level) of an input to which it is connected, causing multiple transitions.

Other outputs in the same device may also be affected because the output voltages are referred to the internal device ground. The ringing causes this internal ground to move away from external ground. The other LOW outputs are connected to the internal ground through a low-impedance transistor, and movement in this ground will

therefore be reflected at these outputs. Again, this may lead to erroneous transitions in devices connected to these outputs. In addition, the movement of the internal ground may corrupt data stored in the registers.

At this point it is worth noting a different effect also caused by parasitic impedances in the power connections. In accordance with industry practice, the output delays of AMD parts are measured with only one output switching. When more than one output switches, the impedance in the common power-supply connections reduces the current available to each output, thus increasing the delay. This effect occurs in any integrated circuit.

THE SOLUTION

The effects of the load capacitance and the interconnection parasitics are inescapable, although the latter may be minimized by good chip design. The solution must lie in modifying the pull-down transistor.

The AMD solution structures the pull-down transistor so it limits the initial current minimizing the transient; then, after a delay, its strength increases to provide sufficient current to maintain the LOW logic level. This is achieved by using two transistors contained in parallel output buffers. These buffers are designed to have different drive capabilities. One has small transistors with low drive which is used to initiate the transition without causing the shock excitation. After a short delay, a second larger driver turns on. This driver completes the transition, and is capable of sinking the necessary dc current to maintain V_{OL}. Additionally, a similar parallel structure is used in the pull-up circuit to moderate the LOW-to-HIGH transition.

While introducing delay into a high-speed circuit may appear counter productive, that is not the case. The primary objective must be to achieve a stable output
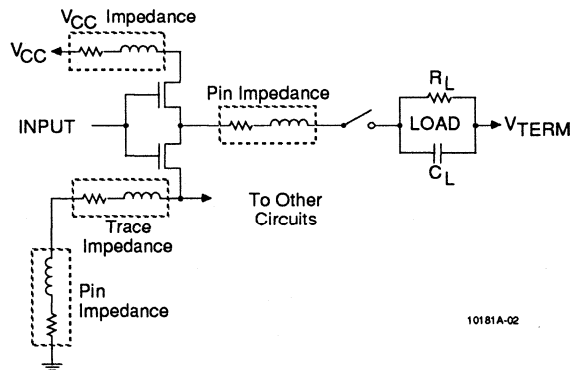
Figure 2. Real Driver and Parasitics

voltage level less than V_{IL} as quickly as possible. The non-controlled output signal may reach V_{IL} sooner, but it will not remain there until the ringing has subsided. This may require more time than the specified output delay, and a good design must allow for this. The modified AMD output will provide a stable, usable voltage level in less time in spite of the added delay.

A secondary effect of limiting the current during transition is that the slew rate is controlled by the driver rather than power-supply parasitics. This generally leads to less delay variations (skew) caused by a different number of switching outputs.

TEST RESULTS

The output driver described above has been incorporated into the Am29C982 4-bit x 4-port Multiple Bus Exchange. This product was mounted in a test jig and its output characteristics photographed. For comparison, a similar test jig was used to test an Am29C821 10-bit register, with traditional 24 mA totem-pole outputs, and a competitive 48 mA output version.

The jigs were designed to eliminate, as far as possible, electrical effects due to the mounting and probing so that intrinsic characteristics of the IC could be observed. It should be noted that the layout and dc loading found on a carefully designed pc board could lower the current transient and its effects. In that respect the following results should be considered worst case.

The test jigs were constructed of double-sided copper-clad board. The two copper planes were used for V_{cc} and GND. Holes were drilled to accept the ICs, and only sufficient copper was cut away to allow clearance of active pins. The ICs were soldered directly into this board. Decoupling was provided by a tantalum capacitor, and a .01 µF ceramic capacitor mounted close to the V_{cc} pin.

Each output was loaded with 47 pF to GND. The leads of this capacitor were cropped short, and the capacitor was soldered directly to the IC pin and the ground plane. Outputs to be observed were connected to SMB sockets through 453 Ω resistors. Each series resistor, together with a 50 Ω oscilloscope input imped-ance, creates a standard 500 Ω load. The leads of each resistor were cropped short and soldered directly to the IC pin and the socket. The socket body was soldered to the ground plane.

These SMB sockets were connected by coax to the 50 Ω oscilloscope input (Tektronix 7854 with 7S14 sampling input plug-in). The series resistance creates an attenu-ation of 10:1. The vertical scale is 2 V/div, and the horizontal scale is 20 ns/div.

On the Am29C821, input D_0 was grounded to provide a "quiet" output Y_0. Y_0 was chosen, because it is farthest from the ground pin, and therefore, most susceptible to noise in the supply. Inputs D_{1-9} were all connected to output Y_8 through a single inverter. The device was then clocked, such that the nine outputs (Y_{1-9}) toggled simul-taneously.

Photograph 1 shows the outputs Y_0 and Y_1 during a HIGH-to-LOW transition. The quiet output (Y_0) "bounces" approximately 2.2 V. The maximum positive ringing in Y_1 is approximately 1.5 V. Observation of the transition on the Y_9 output, which is closer to the GND pin, revealed slightly less ringing.

It should be noted that the capacitive loading of the quiet output reduces the initial transient slope and slightly reduces the positive excursion. Since an actual applica-tion will present capacitive loading, this test is represen-tative. Without the capacitor, the positive excursion was approximately 0.2 V greater.
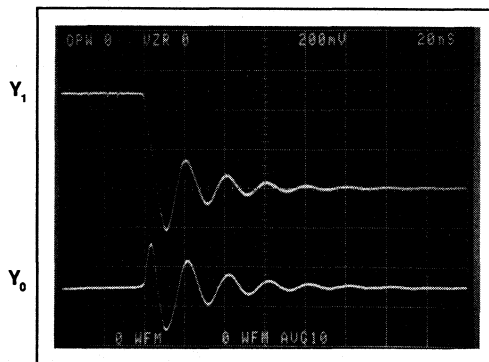
Photo 1. Am29C821

Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.

Photograph 2 shows the same outputs during a LOW-to-HIGH transition. Here the effect is much less; the excursion of Y_0 is approximately 0.9 V. In this case, Y_9, which is farther from V_{CC}, exhibited slightly more ringing.

The same tests were performed on a competitor's version of the Am29C821. The results are shown in photographs 3 and 4. As expected, the 48 mA outputs of this part create considerably more noise than the 24 mA outputs of the AMD part.

To test the Am29C982 Multiple Bus Exchange, the A-port was configured as an input that was directed to the B-, C- and D-Ports which were outputs. A_0 was grounded, and a square wave was applied to A_{1-3}. This again gave nine switching outputs and three quiet outputs.

The outputs on D_0 and D_3 are shown in photographs 5 and 6 for HIGH-to-LOW and LOW-to-HIGH transitions respectively. The effect of the modified output driver is quite clear. Both ringing and ground bounce have been reduced dramatically.

The maximum ground bounce during the negative transition is approximately 1.1 V, while the positive ringing is limited to approximately 0.8 V. When compared to Am29C800, this represents a 50% reduction in noise, while increasing the output current from 24 mA to 48 mA.

The tests on the Am29C982 were repeated with the load capacitors increased to 470 pF. The results are shown in photographs 7 and 8. The amplitude of the ringing and ground bounce are the same or less than with the 47 pF load. The ringing frequency is predictably lower due to the larger capacitor.

The improved output structure is also used in the Am29C983 9-Bit x 4-Port Multiple Bus Exchange. A more comprehensive analysis of this output transition control technique, including results from additional package options and the Am29C983, are being prepared for future release.
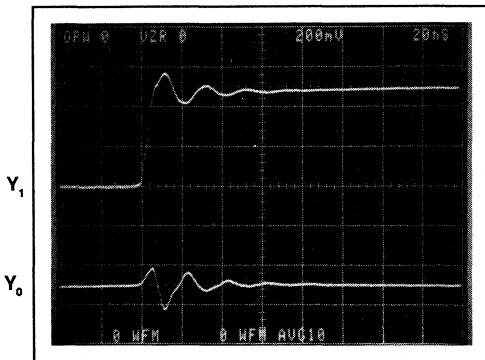
Photo 2. Am29C821
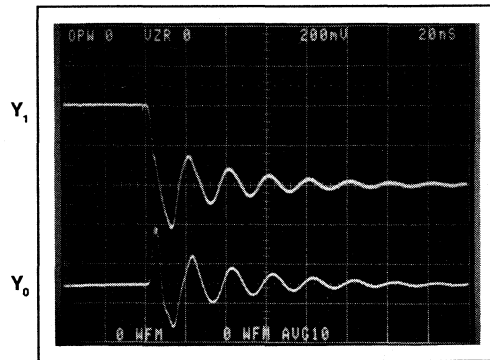
Photo 3. Competitor's C821

Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.
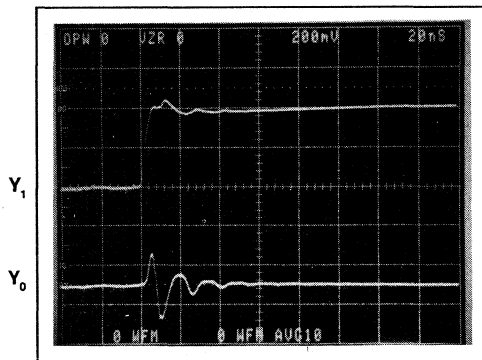
Photo 4. Competitor's C821

While these tests were performed on individual, randomly selected parts, and cannot therefore be considered definitive, they do indicate the effectiveness of the new output structure. It is AMD's intent to incorporate outputs with this improved current characteristic into future bus interface devices.

GOOD DESIGN PRACTICE

Ground bounce cannot be eliminated through good design practice alone. However, the situation can be aggravated considerably by failure to follow good practices. The following guidelines are suggested:

• Ensure good power supply connection. Power supply planes are essential, and wire wrap should be avoided. Provide good wide-band decoupling. The

ringing occurs at very high frequency, in the gigahertz region. Therefore, a comprehensive decoupling scheme should be designed, including chip capacitors very close to the high-drive devices.

• In general, the layout rules followed should be similar to those for ECL. Branching traces should not be used for signals that are to be routed to more than one input. Traces should pass from one input to the next without Ys or Ts. If possible, the traces should have controlled impedance, and should be terminated.
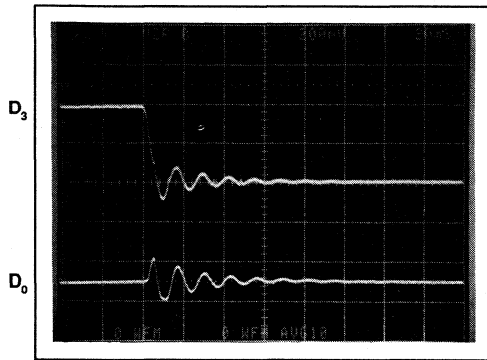
Photo 5. Am29C982
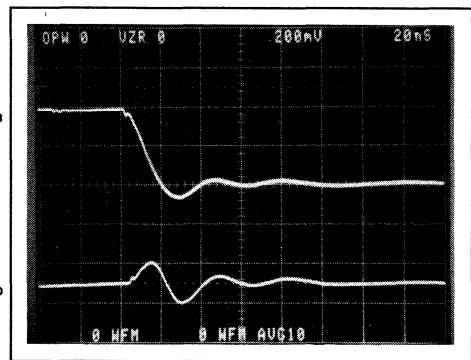
Photo 7. Am29C982 (470 pF)

Photo 6. Am29C982
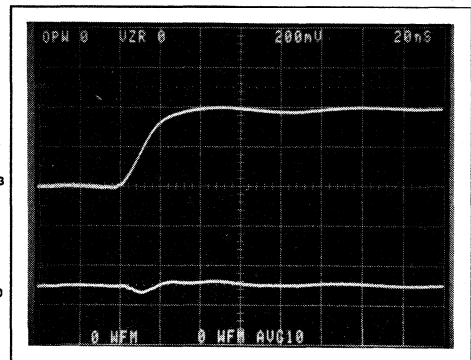
Photo 8. Am29C982 (470 pF)

Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.

CHAPTER 4
Am29C800A Family Data Sheets

Am29C818A

CMOS Pipeline Register with SSR™ Diagnostics

DISTINCTIVE CHARACTERISTICS

■ High-speed noninverting 8-bit parallel register
for any data path or pipelining application

■ WCS (Writable Control Store) pipeline register
– Load WCS from serial register
– Read WCS via serial scan

■ Alternate sourced as SN74ACT818

■ High-speed 8-bit "shadow register" with serial
shift mode for Serial Shadow Register (SSR)
Diagnostics
– Controllability: serial scan in new machine state
– Observability: serial scan out diagnostics routine
results

■ Low standby power

■ JEDEC FCT-compatible specs

GENERAL DESCRIPTION

The Am29C818A is a high-speed, general-purpose
pipeline register with an on-board shadow register for
performing Serial Shadow Register (SSR) Diagnostics
and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path
pipeline register for normal system operation. The
shadow register can load parallel data to or from the
pipeline register and can output data through the D input
port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that se-
lect parallel inputs from the Y-port or adjacent bits in the
shadow register to operate as a shift register. In the se-

rial shift mode, SDI is shifted into the '0' location of the
Shadow register and the contents of '7' location appear
at the SDO output. This register can then participate in a
serial loop throughout the system where normal data,
address, status and control registers are replaced with
Am29C818A Diagnostics Pipeline Registers. The loop
can be used to scan in a complete test routine starting
point (data, address, etc.). Then after a specified num-
ber of clock cycles, the data clocked out can be com-
pared to the expected results. WCS loading can be ac-
complished using the same technique. An instruction
word can be serially shifted into the shadow register and
written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM

09323-001A

CONNECTION DIAGRAMS
Top View

DIPs*

$\overline{OEY}$	1	24	Vcc
DCLK	2	23	MODE
D_0	3	22	Y_0
D_1	4	21	Y_1
D_2	5	20	Y_2
D_3	6	19	Y_3
D_4	7	18	Y_4
D_5	8	17	Y_5
D_6	9	16	Y_6
D_7	10	15	Y_7
SDI	11	14	SDO
GND	12	13	PCLK

09323-002A

PLCC

Top pins: D_0 (4), DCLK (3), $\overline{OEY}$ (2), NC (1), Vcc (28), MODE (27), Y_0 (26)

Left side: D_1 (5), D_2 (6), D_3 (7), NC (8), D_4 (9), D_5 (10), D_6 (11)

Bottom pins: D_7 (12), SDI (13), GND (14), NC (15), PCLK (16), SDO (17), Y_7 (18)

Right side: Y_1 (25), Y_2 (24), Y_3 (23), NC (22), Y_4 (21), Y_5 (20), Y_6 (19)
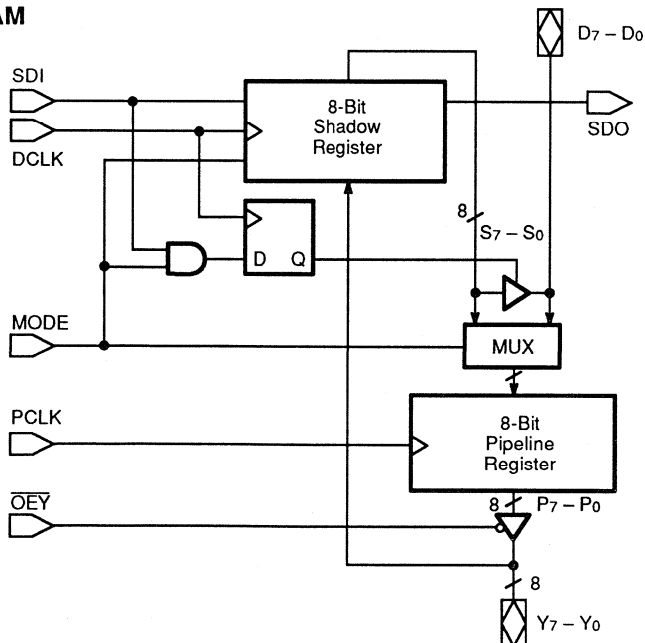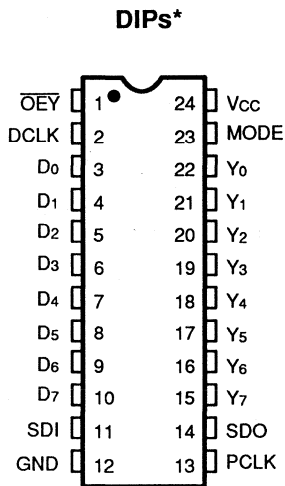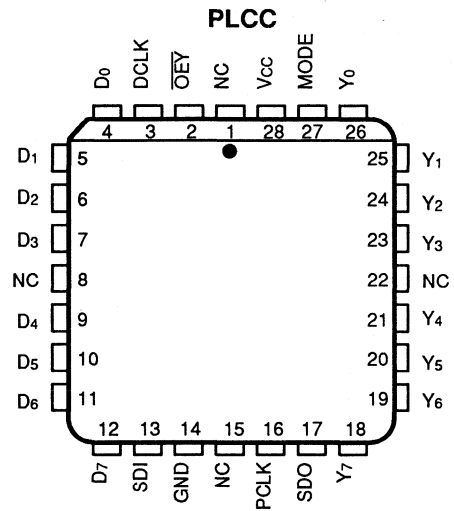
09323-003A

*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

Am29C818A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

```
AM29C818A            P    C
```

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
S = 24-Pin Plastic Small Outline Package (SO 024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C818A
CMOS Pipeline Register with SSR Diagnostics
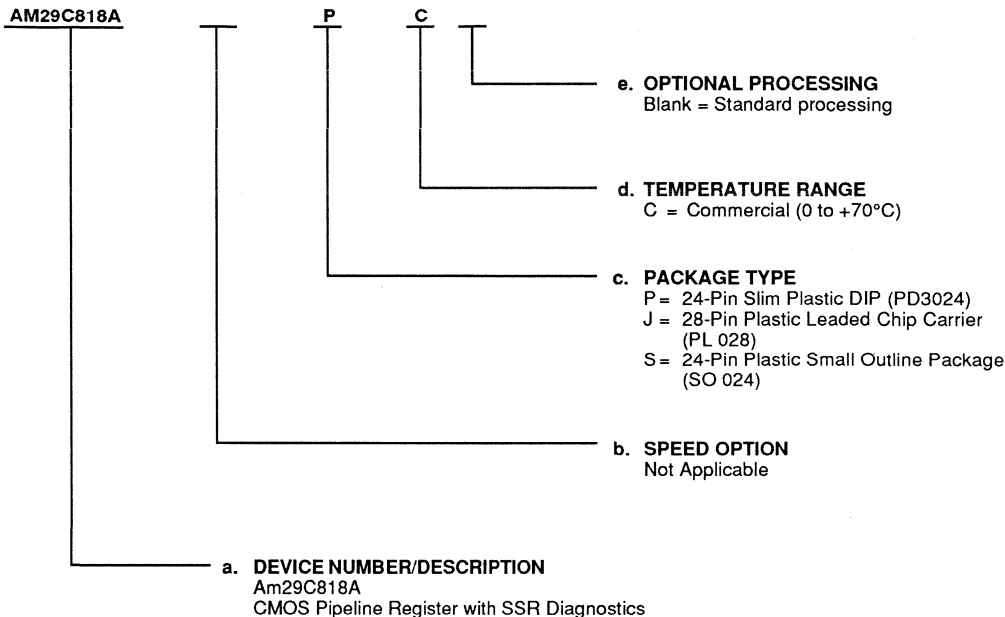
Valid Combinations	
AM29C818A	PC, SC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

    a.   **Device Number**
    b.   **Speed Option (if applicable)**
    c.   **Device Class**
    d.   **Package Type**
    e.   **Lead Finish**

AM29C818A   **/B**   **L**   **A**

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C818A
CMOS Pipeline Register with SSR Diagnostics

Valid Combinations	
AM29C818A	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

       Am29C818A

PIN DESCRIPTION

$D_0 - D_7$

Parallel Data Inputs (Input/Output)

Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK

Diagnostics Clock (Input)

Diagnostics/WCS clock for loading shadow register (serial or parallel modes – see Function Table).

MODE

Mode Control (Input)

Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$

Y-Port Output Enable (Input: Active LOW)

Active LOW output enable for Y-port.

PCLK

Pipeline Register Clock (Input)

Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI

Serial Data Input (Input)

Input to shadow register (see Function Table).

SDO

Serial Data Output (Output)

Output from shadow register.

$Y_0 - Y_7$

Parallel Data Outputs (Input/Output)

Data outputs from the pipeline register and parallel inputs to the shadow register.

FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no setup or hold times are violated, this simultaneous operation is legal.

FUNCTION TABLE

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_0 \leftarrow SDI$	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	SDI	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Reg.
H	H	↑	X	SDI	Hold*	NA	Hold Shadow Register; $D_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

Table Definitions

Inputs

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH Transition

Outputs

$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable, output is not a function of the specified input combinations.

APPLICATIONS
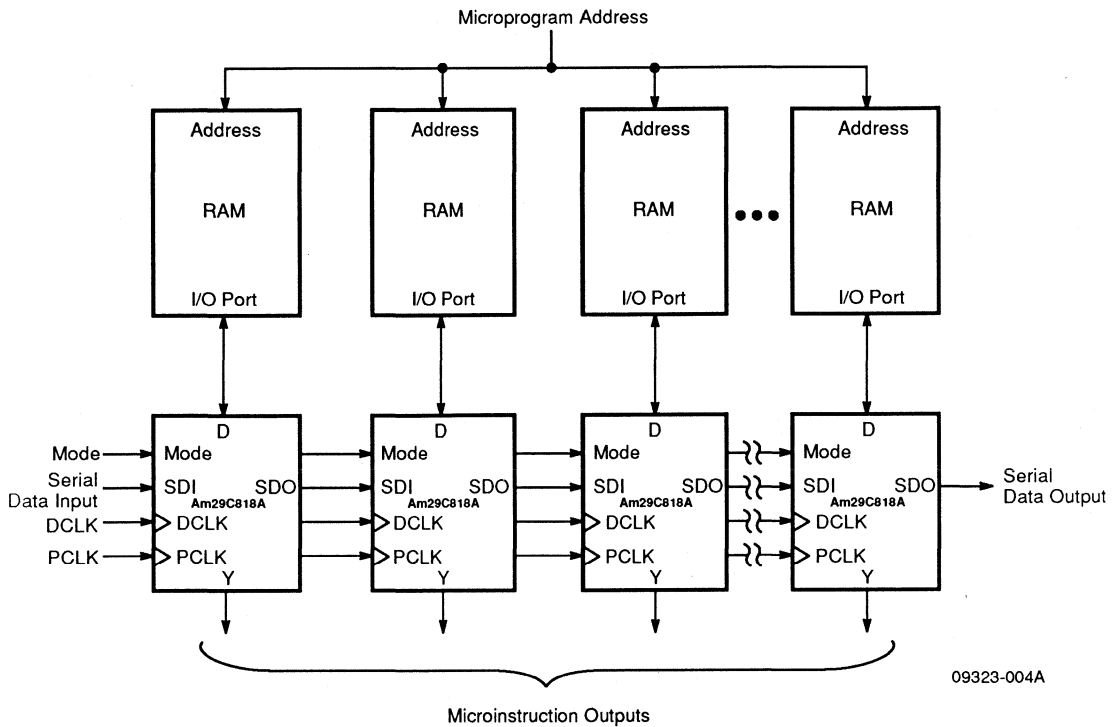
Am29C818A-Based WCS Application

APPLICATIONS (Continued)

Microprogram Address

Microinstruction Outputs
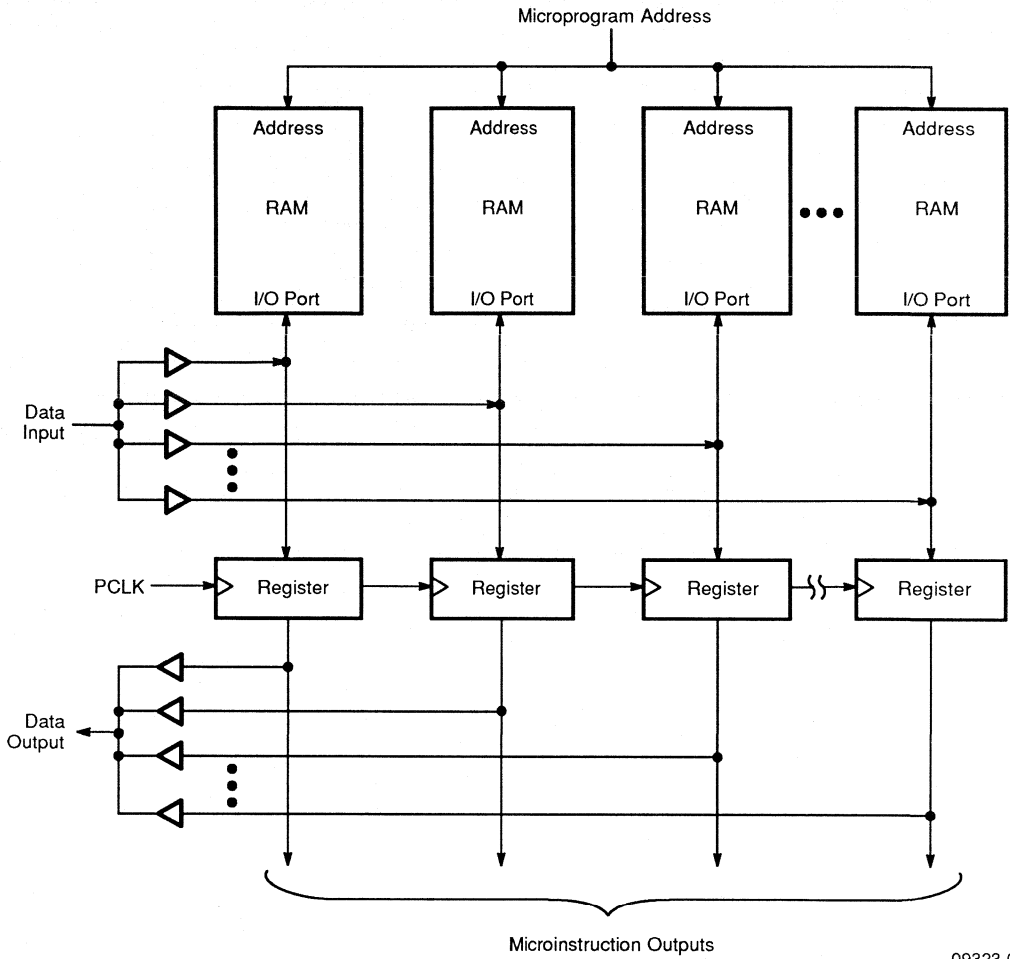
09323-005A

WCS Application without Am29C818As

SHADOW REGISTER

09323-006A

Am29C818A

An Introduction to Serial Shadow Register (SSR) Diagnostics

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both observe intermediate test points and control intermediate signals – address, data, control and status – to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinatorial and Sequential Networks

The problem of testing a combinatorial logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.

09323-007A

Figure 1. Combinatorial Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

09323-008A

Figure 2. Sequential Network

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinatorial network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.

09323-009A

Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with

PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinatorial networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29C818A.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feedback paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29C818A's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

09323-010A

Figure 4. SSR Diagnostics Logical Path
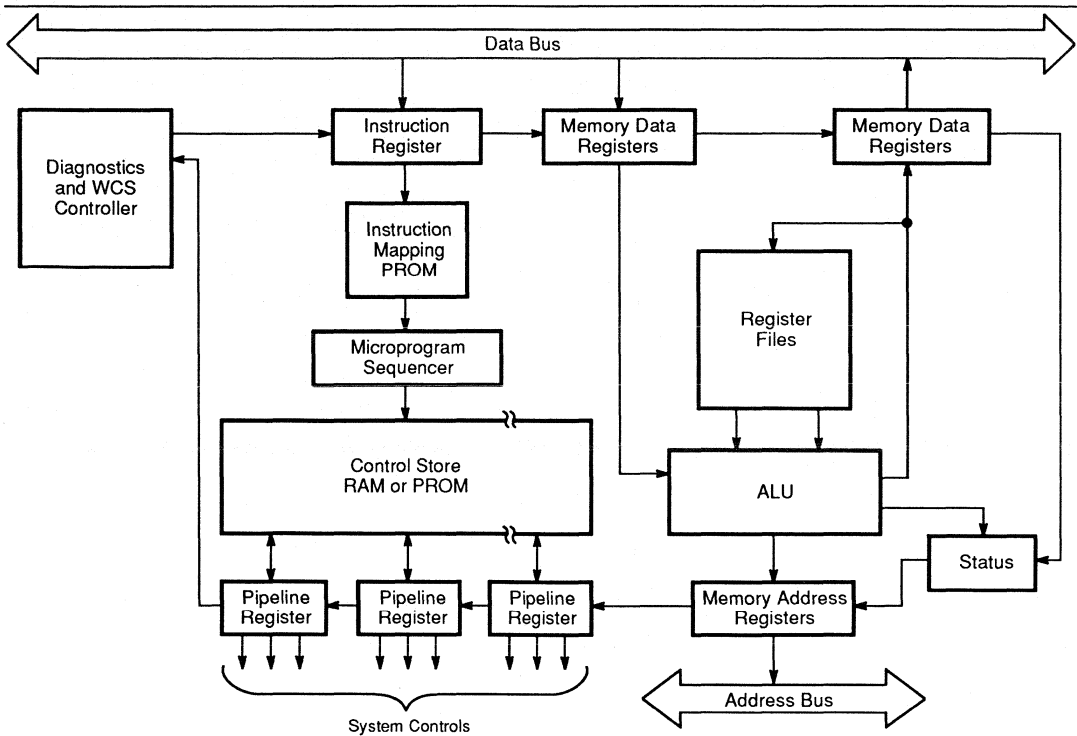
SSR Diagnostics/WCS Pipeline Registers
Replace Normal Registers with Diagnostics Loop

09323-011A

Figure 5. Typical System Configuration

Use of the Am29C818A Pipeline Register in Writable Control Store (WCS) Designs

The Am29C818A SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29C818A supports all of the above operations (and more) without any support circuitry. Figure 6 shows

a typical WCS design with the Am29C818A. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinatorial network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.
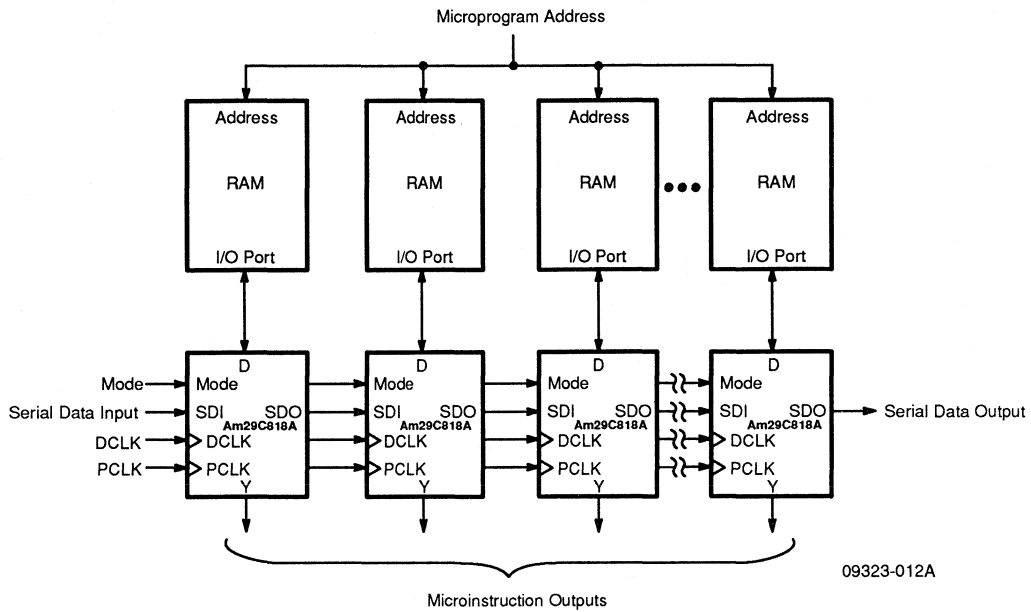
Figure 6. Am29C818A-Based WCS Application
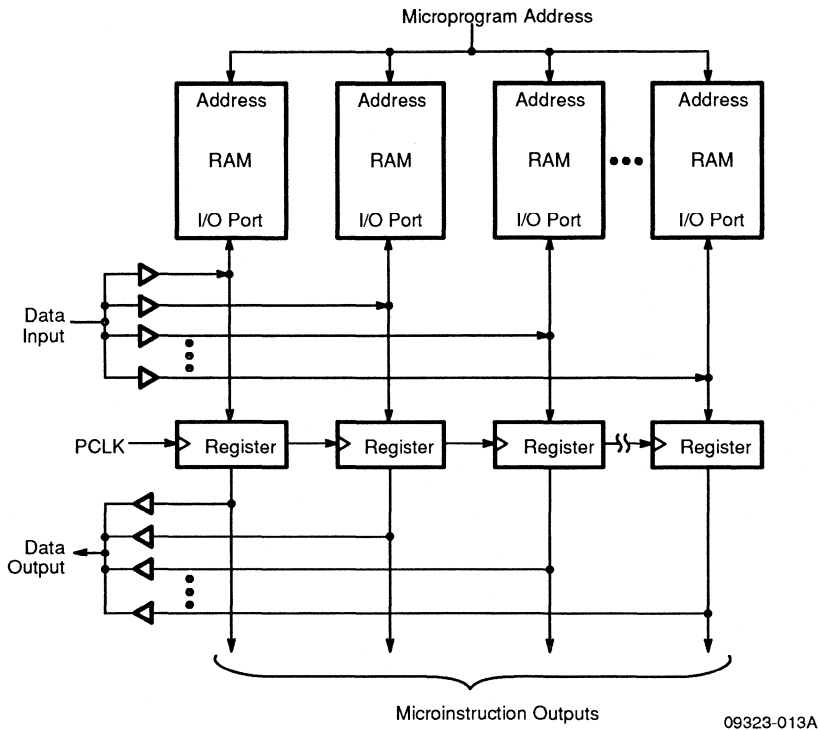
Figure 7. WCS Application without Am29C818As

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	$-65°C$ to $+150°C$
Supply Voltage to Ground Potential Continuous	-0.5 V to $+7.0$ V
DC Output Voltage	-0.5 V to $+6.0$ V
DC Input Voltage	-0.5 V to $+6.0$ V

DC Output Diode Current:

Into Output	$+50$ mA
Out of Output	-50 mA

DC Input Diode Current:

Into Input	$+20$ mA
Out of Input	-20 mA

DC Output Current per Pin:

Into Output	$+48$ mA ($2 \times I_{OL}$)
Out of Output	-30 mA ($2 \times I_{OH}$)

Total DC Ground Current
($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)

Total DC V_{CC} Current
($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to $+70°C$
Supply Voltage (V_{CC})	$+4.5$ V to $+5.5$ V

Military (M) Devices

Temperature (T_A)	-55 to $+125°C$
Supply Voltage (V_{CC})	$+4.5$ V to $+5.5$ V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 4.5$ V	Y_0–Y_7	$I_{OH} = -15$ mA	2.4		V
		$V_{IN} = V_{IH}$ or V_{IL}	D_0–D_7, SDO	$I_{OH} = -3$ mA	2.4		
V_{OL}	Output LOW Voltage	$V_{CC} = 4.5$ V	Y_0–Y_7	$I_{OL} = 24$ mA		0.5	V
		$V_{IN} = V_{IH}$ or V_{IL}	D_0–D_7, SDO	$I_{OL} = 8.0$ mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)			2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	V
V_{IC}	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA				−1.2	V
I_{IL}	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = $ GND				−10	µA
I_{IH}	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V				10	µA
I_{OZH}	Output Off-State Current (High-Impedance)	$V_{CC} = 5.5$ V	$V_O = V_{CC}$			20	µA
I_{OZL}		$V_{CC} = 5.5$ V	$V_O = $ GND			−20	µA
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.5$ V, $V_{OUT} = 0$ V (Note 2)		Y_0–Y_7	−60		mA
				D_0–D_7, SDO	−20		
I_{CCQ}	Static Supply Current	$V_{CC} = 5.5$ V Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL		1.5	µA
				COM'L		1.2	
I_{CCT}			$V_{IN} = 3.4$ V	D_x, Y_x		1.5	mA/Bit
				$\overline{OEY}$, DCLK, SDI, MODE, PCLK		3.0	
I_{CCD}†	Dynamic Supply Current	$V_{CC} = 5.5$ V (Note 3)				400	µA/MHz/Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.
† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Commercial Min.	Commercial Max.	Military Min.	Military Max.	Unit
t_{PLH} & t_{PHL}	PCLK → Yx			12		14	ns
	MODE → SDO			12		14	ns
	SDI → SDO			12		14	ns
	DCLK → SDO			16		18	ns
t_S	Dx → PCLK		4		6		ns
	MODE → PCLK		6		8		ns
	Yx → DCLK		6		8		ns
	MODE → DCLK	C_L = 50 pF	6		8		ns
	SDI → DCLK	$R_1 = R_2 = 500\ \Omega$	6		8		ns
	DCLK → PCLK		20		20		ns
	PCLK → DCLK		20		20		ns
t_H	Dx → PCLK		2		2		ns
	MODE → PCLK		2		2		ns
	Yx → DCLK		2		2		ns
	MODE → DCLK	See Test Output Load Conditions	2		2		ns
	SDI → DCLK		2		2		ns
t_{LZ}	$\overline{OEY}$ → Yx			12		14	ns
	DCLK → Dx			14		16	ns
t_{HZ}	$\overline{OEY}$ → Yx			12		14	ns
	DCLK → Dx			14		16	ns
t_{ZL}	$\overline{OEY}$ → Yx			14		16	ns
	DCLK → Dx			18		20	ns
t_{ZH}	$\overline{OEY}$ → Yx			14		16	ns
	DCLK → Dx			18		20	ns
t_{PW}	PCLK (HIGH and LOW)		8		10		ns
	DCLK (HIGH and LOW)		8		10		ns

Am29C821A/Am29C823A

High-Performance CMOS Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots and ground bounce**
- **High-speed parallel positive edge-triggered registers with D-type flip-flops**
  - CP-Y propagation delay = 5 ns typical
- **Low standby power**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military

- **Extra-wide (9- and 10-bit) data paths**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **Minimal speed degradation with multiple outputs switching**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C821A and Am29C823A CMOS Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A registers are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C821A is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823A is a 9-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821A and Am29C823A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry, which utilizes n-channel pull-up transistors (eliminating the parasitic diode to Vcc), provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C821A and Am29C823A are available in the standard package options: DIPs, PLCCs, and SOICs.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

BLOCK DIAGRAMS
Am29C821A
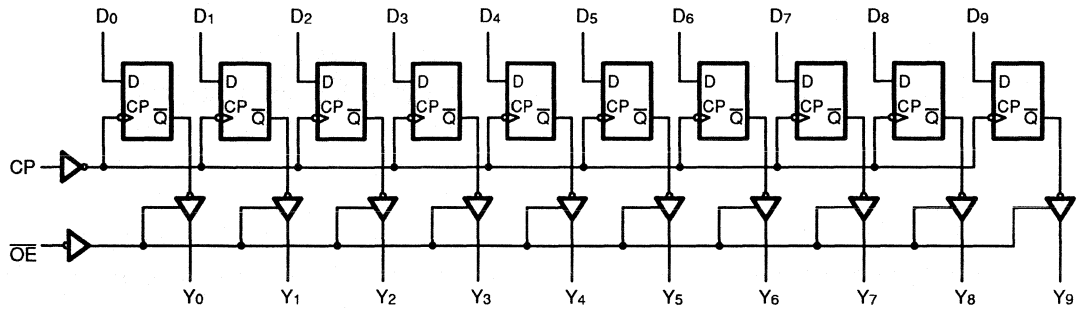
11227-001A

Am29C823A

11227-002A

CONNECTION DIAGRAMS (Top View)
Am29C821A

DIP*

```
 OE  [ 1●     24 ]  Vcc
 D0  [ 2      23 ]  Y0
 D1  [ 3      22 ]  Y1
 D2  [ 4      21 ]  Y2
 D3  [ 5      20 ]  Y3
 D4  [ 6      19 ]  Y4
 D5  [ 7      18 ]  Y5
 D6  [ 8      17 ]  Y6
 D7  [ 9      16 ]  Y7
 D8  [ 10     15 ]  Y8
 D9  [ 11     14 ]  Y9
 GND [ 12     13 ]  CP
```

PLCC

Top pins: D_1 (4), D_0 (3), $\overline{OE}$ (2), NC (1), V_{CC} (28), Y_0 (27), Y_1 (26)

```
 D2  [ 5              25 ]  Y2
 D3  [ 6              24 ]  Y3
 D4  [ 7              23 ]  Y4
 NC  [ 8              22 ]  NC
 D5  [ 9              21 ]  Y5
 D6  [ 10             20 ]  Y6
 D7  [ 11             19 ]  Y7
```

Bottom pins: D_8 (12), D_9 (13), GND (14), NC (15), CP (16), Y_9 (17), Y_8 (18)

11227-003A

11227-004A

Am29C823A

DIP*

```
 OE  [ 1●     24 ]  Vcc
 D0  [ 2      23 ]  Y0
 D1  [ 3      22 ]  Y1
 D2  [ 4      21 ]  Y2
 D3  [ 5      20 ]  Y3
 D4  [ 6      19 ]  Y4
 D5  [ 7      18 ]  Y5
 D6  [ 8      17 ]  Y6
 D7  [ 9      16 ]  Y7
 D8  [ 10     15 ]  Y8
 CLR [ 11     14 ]  EN
 GND [ 12     13 ]  CP
```

PLCC

Top pins: D_1 (4), D_0 (3), $\overline{OE}$ (2), NC (1), V_{CC} (28), Y_0 (27), Y_1 (26)

```
 D2  [ 5              25 ]  Y2
 D3  [ 6              24 ]  Y3
 D4  [ 7              23 ]  Y4
 NC  [ 8              22 ]  NC
 D5  [ 9              21 ]  Y5
 D6  [ 10             20 ]  Y6
 D7  [ 11             19 ]  Y7
```

Bottom pins: D_8 (12), $\overline{CLR}$ (13), GND (14), NC (15), CP (16), $\overline{EN}$ (17), Y_8 (18)
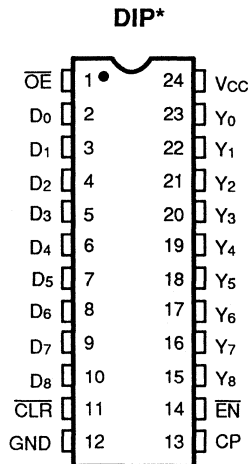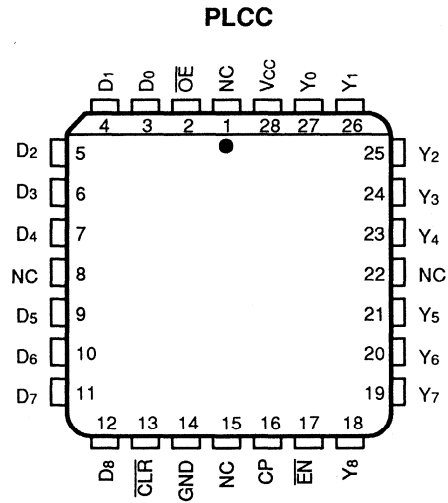
11227-005A

11227-006A

*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

LOGIC SYMBOLS

Am29C821A   Am29C823A
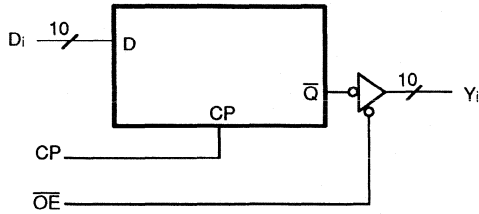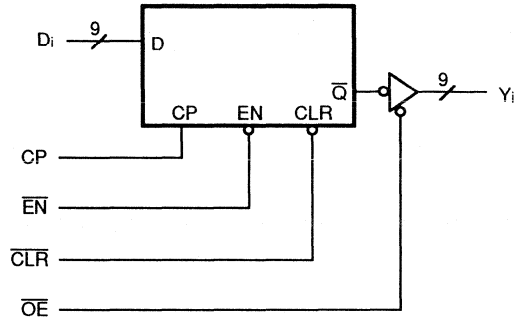
11227-007A   11227-008A

FUNCTION TABLES

Am29C821A

Inputs			Internal	Outputs	
$\overline{OE}$	D_i	CP	$\overline{Q}_i$	Y_i	Function
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Am29C823A

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	Function
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

H = HIGH   NC = No Change

L= LOW   ↑ = LOW-to-HIGH Transition

X = Don't Care   Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

AM29C821A
AM29C823A
                P   C

e. OPTIONAL PROCESSING
    Blank = Standard processing

d. TEMPERATURE RANGE
    C = Commercial (0 to +70°C)

c. PACKAGE TYPE
    P = 24-Pin Slim Plastic DIP (PD3024)
    S = 24-Pin Plastic Small Outline Package (SO 024)
    J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. SPEED OPTION
    Not Applicable

a. DEVICE NUMBER/DESCRIPTION
    Am29C821A CMOS 10-Bit Register
    Am29C823A CMOS 9-Bit Register

Valid Combinations	
AM29C821A	PC, SC, JC
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

    a. **Device Number**
    b. **Speed Option (if applicable)**
    c. **Device Class**
    d. **Package Type**
    e. **Lead Finish**

AM29C821A
AM29C823A   /B L A

e. **LEAD FINISH**
   A = Hot Solder Dip

d. **PACKAGE TYPE**
   L = 24-Pin Slim Ceramic DIP (CD3024)

c. **DEVICE CLASS**
   /B = Class B

b. **SPEED OPTION**
   Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**
   Am29C821A CMOS 10-Bit Register
   Am29C823A CMOS 9-Bit Register

Valid Combinations	
AM29C821A	/BLA
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION
Am29C821A/Am29C823A

D_i
Data Input (Input)

D_i are the register data inputs.

CP
Clock Pulse (Input, LOW-to-HIGH Transition)

Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

Y_i
Data Outputs (Output)

Y_i are the three-state outputs.

$\overline{OE}$
Output Enable (Input, Active LOW)

When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is present at the Y_i outputs.

Am29C823A only

$\overline{EN}$
Clock Enable (Input, Active LOW)

When $\overline{EN}$ is LOW, data on the Di inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of the data or clock input transitions.

$\overline{CLR}$
Clear (Input, Active LOW)

When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the $\overline{Q}_i$ outputs are HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

StorageTemperature	−65 to +150°C
Supply Voltage to Ground Potential Continous	−0.5 V to +7.0 V
DC Output Voltage	−0.5 V to +6.0 V
DC Input Voltage	−0.5 V to +6.0 V

DC Output Diode Current:
Into Output	+50 mA
Out of Output	−50 mA

DC Input Diode Current:
Into Input	+20 mA
Out of Input	−20 mA

DC Output Current:
Into Output	+100 mA
Out of Output	−100 mA

Total DC Ground Current
$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)

Total DC V_{CC} Current
$(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Military (M) Devices
Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified
(for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V $V_{IN} = V_{IH}$ or V_{IL}	MIL I_{OL} = 32 mA		0.5	V
			COM'L I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = –18 mA			–1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND			–5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V			+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = GND			–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)		–60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	$V_{IN} = V_{CC}$ or GND · MIL		1.5	mA
			COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V · Data Input		1.5	mA/ Bit
			$\overline{OE}, \overline{CLR}, CP, \overline{EN}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)	Outputs Open		275	µA/ MHz/ Bit
			Outputs Loaded		400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.

2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.

3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

Am29C821A/AM29C823A

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description	Test Conditions*		Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i			2	8.5	2	9.5	ns
t_{PHL}	($\overline{OE}$ = LOW) (Note 1)			3	8.5	3	9.5	ns
t_s	Data to CP Setup Time			3		3		ns
t_H	Data to CP Hold Time			2		2		ns
t_s	Enable ($\overline{EN}$ ⌐L) to CP Setup Time			4		4		ns
t_s	Enable ($\overline{EN}$ ⌐⌐) to CP Setup Time			4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time	C_L = 50 pF		0		0		ns
t_{PHL}	Propagation Delay, Clear to Y_i	R_1 = 500 Ω		3	10	3	10.5	ns
t_{REC}	Clear ($\overline{CLR}$ ⌐⌐) to CP Setup Time	R_2 = 500 Ω		6		6		ns
t_{PWH}	Clock Pulse Width	HIGH		6		6		ns
t_{PWL}		LOW		6		6		ns
t_{PWL}	Clear Pulse Width	LOW		6		6		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐L to Y_i			1	8.5	1	9	ns
t_{ZL}				3	12	3	13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐⌐ to Y_i			2	8	2	8.5	ns
t_{LZ}				2	8	2	8.5	ns

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 2)

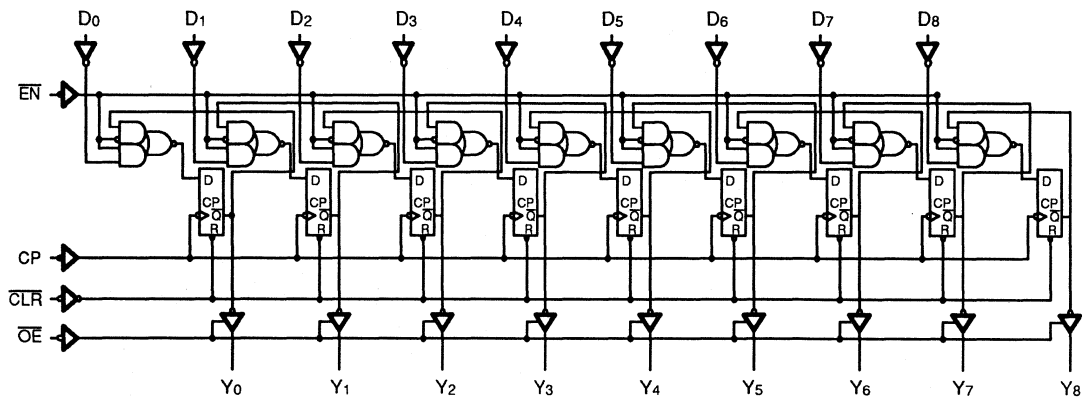| Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i	C_L = 300 pF	2	15.5	2	17.5	ns
t_{PHL}	($\overline{OE}$ = LOW) (Note 1)	R_1 = 500 Ω	3	15.5	3	17.5	ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐L to Y_i	R_2 = 500 Ω	2	15	2	15.5	ns
t_{ZL}			3	18.5	3	19.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐⌐ to Y_i	C_L = 5 pF	2	6.5	2	7	ns
t_{LZ}		R_1 = 500 Ω R_2 = 500 Ω	2	6.5	2	7	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

2. These parameters are guaranteed by characterization but not production tested.

Am29C827A/Am29C828A

High-Performance CMOS Bus Buffers

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS buffers and inverters**
  - D-Y delay = 4 ns typical
- **Low standby power**
- **JEDEC FCT-compatible specs**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military
- **Extra-wide (10-bit) data paths**
- **200-mV typical hysteresis on data input ports**
- **Minimal speed degradation with multiple outputs switching**

- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Ideal for driving 1Mbit x 1 and 1Mbit x 4 DRAM address inputs**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C827A and Am29C828A CMOS Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature 10-bit wide data paths and NORed output enables for maximum control flexibility. The Am29C827A has non-inverting outputs, while the Am29C828A has inverting outputs. Each device has data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C827A and Am29C828A are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 4 ns, as well as an output current drive of 48 mA.

The 29C827A and Am29C828A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By con-

trolling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits or edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C827A and Am29C828A are available in the standard package options: DIPs, PLCCs, and SOICs.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
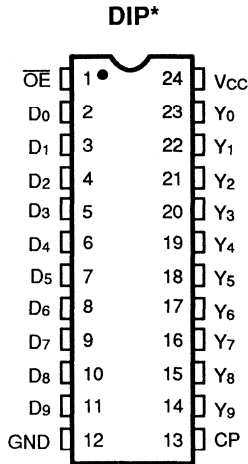
BLOCK DIAGRAMS
Am29C827A (Noninverting)
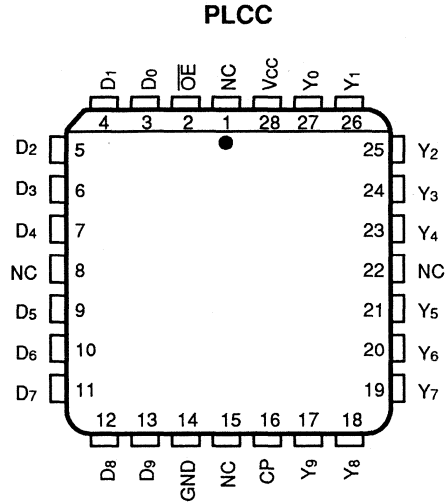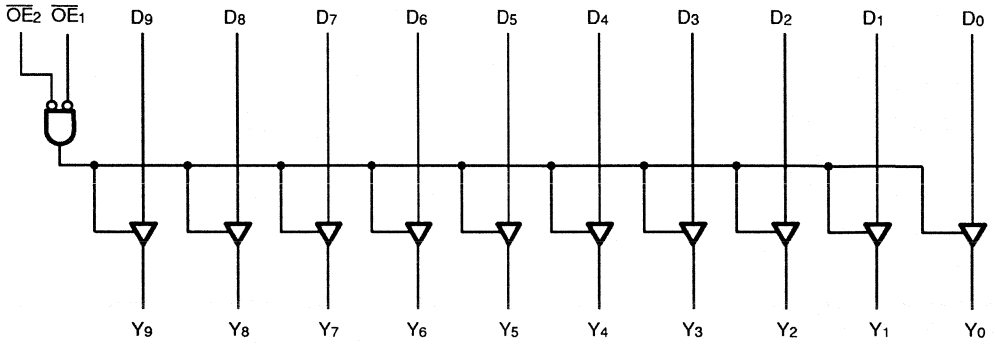

11228-001A

Am29C828A (Inverting)

11228-002A

CONNECTION DIAGRAMS
(Top View)

DIPs*

```
      ┌──┐  ┌──┐
OE  [ 1 •   24 ] Vcc
D0  [ 2     23 ] Y0
D1  [ 3     22 ] Y1
D2  [ 4     21 ] Y2
D3  [ 5     20 ] Y3
D4  [ 6     19 ] Y4
D5  [ 7     18 ] Y5
D6  [ 8     17 ] Y6
D7  [ 9     16 ] Y7
D8  [ 10    15 ] Y8
D9  [ 11    14 ] Y9
GND [ 12    13 ] OE2
```

PLCC

```
        D1  D0  OE1  NC  Vcc  Y0  Y1
         4   3   2   1   28  27  26
D2  [ 5                          25 ] Y2
D3  [ 6                          24 ] Y3
D4  [ 7                          23 ] Y4
NC  [ 8                          22 ] NC
D5  [ 9                          21 ] Y5
D6  [ 10                         20 ] Y6
D7  [ 11                         19 ] Y7
        12  13  14  15  16  17  18
        D8  D9  GND  NC  OE2  Y9  Y8
```
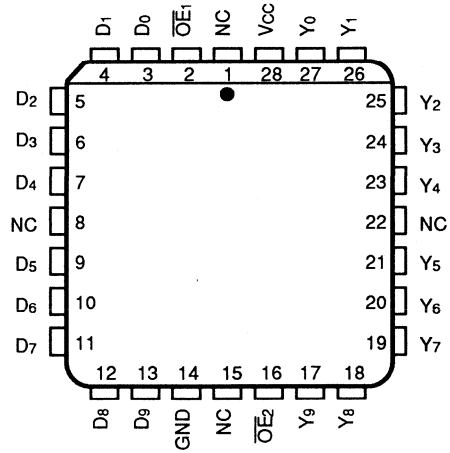
11228-003A

11228-004A

*Also available in Small Outline package; pinout identical to DIPs.

Am29C827A/Am29C828A

LOGIC SYMBOLS

Am29C827A
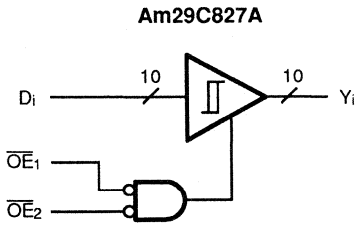
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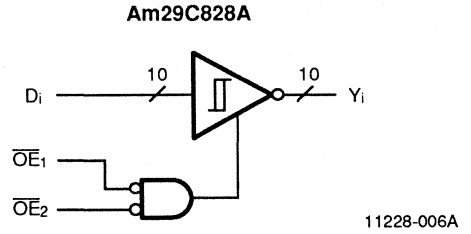
Am29C828A

11228-006A

FUNCTION TABLES

Am29C827A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

Am29C828A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = Hi-Z

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. **Device Number**
    b. **Speed Option (if applicable)**
    c. **Package Type**
    d. **Temperature Range**
    e. **Optional Processing**

```
AM29C827A
AM29C828A          P   C
```

e. **OPTIONAL PROCESSING**
    Blank = Standard processing

d. **TEMPERATURE RANGE**
    C = Commercial (0 to +70°C)

c. **PACKAGE TYPE**
    P = 24-Pin (300-mil) Plastic DIP (PD3024)
    S = 24-Pin Plastic Small Outline Package
        (SO 024)
    J = 28-Pin Plastic Leaded Chip Carrier
        (PL 028)

b. **SPEED OPTION**
    Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**
    Am29C827A
    CMOS 10-Bit Noninverting Buffer

    Am29C828A
    CMOS 10-Bit Inverting Buffer
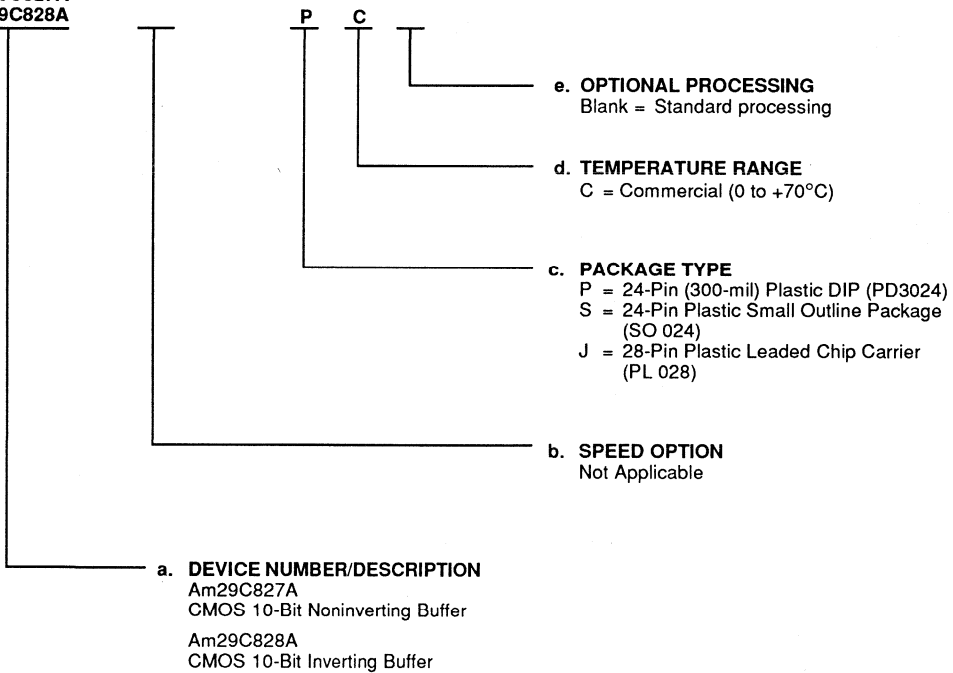
Valid Combinations	
AM29C827A	PC, SC, JC
AM29C828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

    a. **Device Number**
    b. **Speed Option (if applicable)**
    c. **Device Class**
    d. **Package Type**
    e. **Lead Finish**

```
AM29C827A
AM29C828A              /B    L    A
```

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C827A
CMOS 10-Bit Noninverting Buffer

Am29C828A
CMOS 10-Bit Inverting Buffer

Valid Combinations	
AM29C827A	/BLA
AM29C828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$\overline{OE}_i$
Output Enables (Input, Active LOW)

When the $\overline{OE}_1$ and $\overline{OE}_2$ are both LOW, the outputs are enabled. When either one or both are HIGH, the outputs are in the Hi-Z state.

D_i
Data Inputs (Input)

D_i are the 10-bit data inputs.

Y_i
Data Outputs (Output)

Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C

Supply Voltage to Ground Potential

Continuous	−0.5 V to +7.0 V
DC Output Voltage	−0.5 V to +6.0 V
DC Input Voltage	−0.5 V to +6.0 V

DC Output Diode Current:

Into Output	+50 mA
Out of Output	−50 mA

DC Input Diode Current:

Into Input	+20 mA
Out of Input	−20 mA

DC Output Current per Pin:

Into Output	+100 mA
Out of Output	−100 mA

Total DC Ground Current
$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)

Total DC V_{CC} Current
$(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified
### (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15$ mA		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or V_{IL}	MIL $I_{OL} = 32$ mA			0.5	V
			COM'L $I_{OL} = 48$ mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA				−1.2	V
I_{IL}	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = $ GND				−5	µA
I_{IH}	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V				5	µA
I_{OZH}	Output Off-State Current (High Impedance)	$V_{CC} = 5.5$ V, $V_O = 5.5$ V				+10	µA
I_{OZL}		$V_{CC} = 5.5$ V, $V_O = $ or GND				−10	µA
I_{SC}	Output Short-Circuit Current	$V_{CC} = 5.5$ V, $V_O = 0$ V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	$V_{CC} = 5.5$ V Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			$V_{IN} = 3.4$ V	Data Input		1.5	mA/ Bit
				$\overline{OE}_1, \overline{OE}_2$		3.0	
I_{CCD}†	Dynamic Supply Current	$V_{CC} = 5.5$ V (Note 3)	Outputs Open			275	µA/ MHz/ Bit
			Outputs Loaded			400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.

2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.

3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

Am29C827A/Am29C828A

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i)		1.0	7.5	1.0	8.5	ns
t_{PHL}	Am29C827A (Noninverting) (Note 1)		1.0	7.5	1.0	8.5	ns
t_{PLH}	Data (D_i) to Output (Y_i)	C_L = 50 pF	1.0	7.5	0.5	8.5	ns
t_{PHL}	Am29C828A (Inverting) (Note 1)	R_1 = 500 Ω	1.0	7.5	0.5	8.5	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	R_2 = 500 Ω	1.0	9	1.0	11	ns
t_{ZL}			3.0	12	3.0	14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i		2.0	8	2.0	9	ns
t_{LZ}			2.0	8	2.0	9	ns

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified

Symbol	Parameter Description (Note 2)	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i)		1.0	15.5	1.0	17.0	ns
t_{PHL}	Am29C827A (Noninverting) (Note 1)		1.0	15.5	1.0	17.0	ns
t_{PLH}	Data (D_i) to Output (Y_i)	C_L = 300 pF	1.0	13.5	0.5	15.0	ns
t_{PHL}	Am29C828A (Inverting) (Note 1)	R_1 = 500 Ω R_2 = 500 Ω	1.0	14	0.5	15.0	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i		1.0	13.5	1.0	15.0	ns
t_{ZL}			3.0	17	3.0	18.0	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5 pF	2.0	7	2.0	8	ns
t_{LZ}		R_1 = 500 Ω R_2 = 500 Ω	2.0	7	2.0	8	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

2. These parameters are guaranteed by characterization but not production tested.

Am29C833A/Am29C853A

High-Performance CMOS Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS bidirectional bus transceivers**
  - T-R delay = 5 ns typical
  - R-Parity delay = 8 ns typical
- **Error flag with open-drain output**
- **Generates odd parity for all-zero protection**
- **Low standby power**
- **200 mV typical input hysteresis on input data ports**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military

- **Proprietary edge-rate controlled outputs dramatically reduce ground bounce, overshoots and undershoots**
- **Power up/down disable circuit provides for glitch-free power supply sequencing**
- **Minimal speed degradation with multiple outputs switching**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C833A and Am29C853A are high-performance CMOS parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with the ERR flag showing the results of the parity test. Each of these devices is produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 5 ns, as well as an output current drive of 48 mA.

In the Am29C833A, the error flag is clocked and stored in a register which is read at the open-drain ERR output, the CLR input is used to clear the error flag register. In the Am29C853A, a latch replaces this register, and the EN and CLR controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29C833A and Am29C853A, parity logic defaults to the transmit mode, so that the ERR pin reflects the parity of the R port.

The output enables, OER and OET, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user

can force a parity error by enabling both OER and OET simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29C833A and Am29C853A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), overshoots and undershoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuit provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C833A and Am29C853A are available in the standard package options: DIPs, PLCCs, and SOICs.
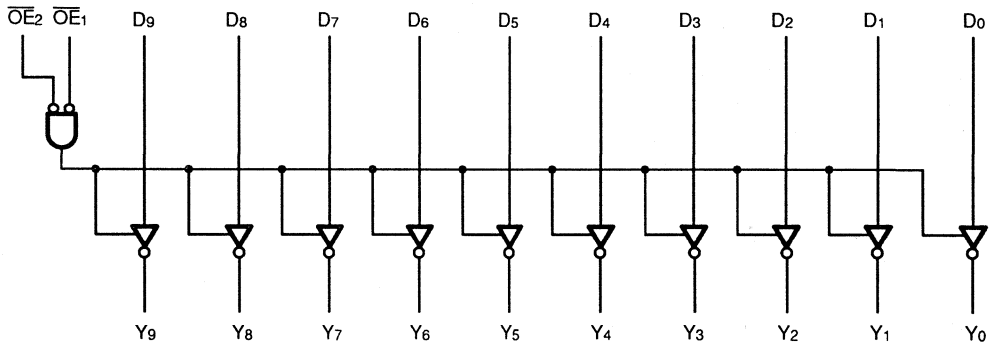
* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
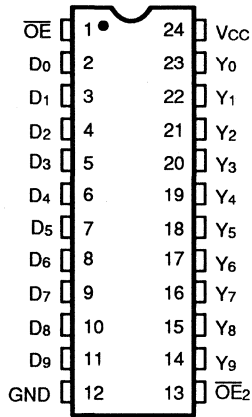
LOGIC SYMBOLS
Am29C833A

11229-001A
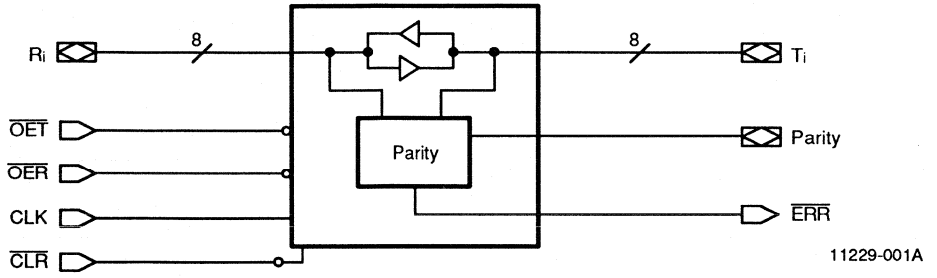
Am29C853A
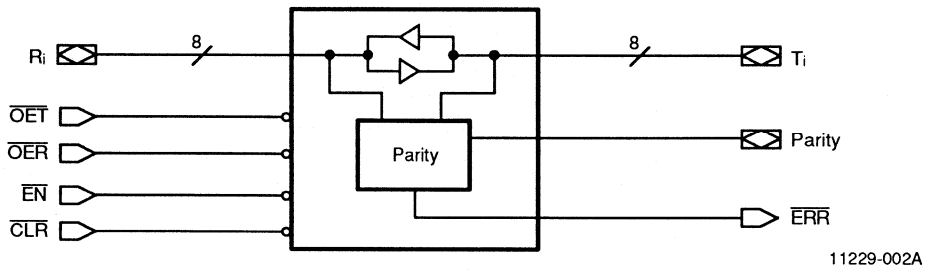
11229-002A

BLOCK DIAGRAMS
Am29C833A
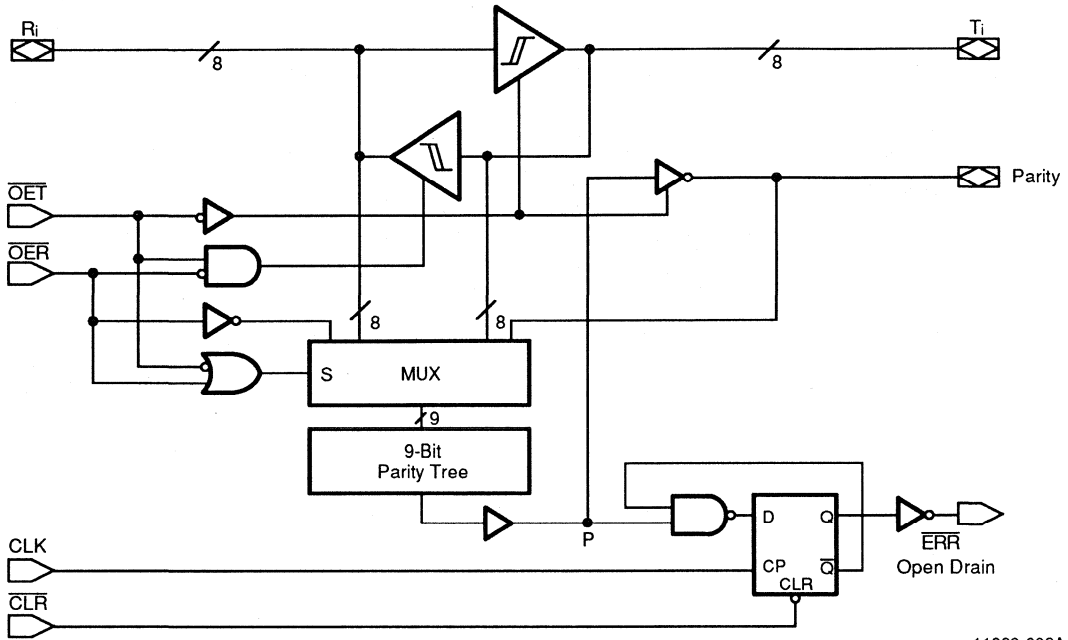
11229-003A

Am29C853A
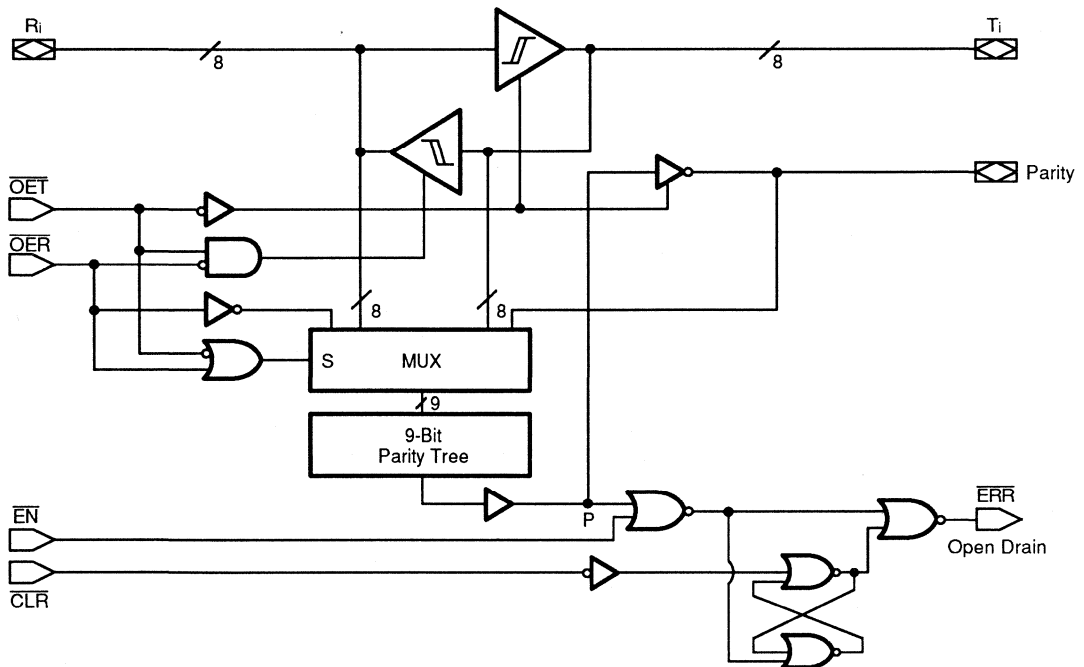
11229-004A

CONNECTION DIAGRAMS (Top View)
Am29C833A

DIPs*

```
      ___
OER [ 1●    24 ] Vcc
 R0 [ 2     23 ] T0
 R1 [ 3     22 ] T1
 R2 [ 4     21 ] T2
 R3 [ 5     20 ] T3
 R4 [ 6     19 ] T4
 R5 [ 7     18 ] T5
 R6 [ 8     17 ] T6
 R7 [ 9     16 ] T7
ERR [ 10    15 ] Parity
CLR [ 11    14 ] OET
GND [ 12    13 ] CLK
```

11229-005A

PLCC

```
         R1  R0  OER  NC  Vcc  T0  T1

          4   3   2   1   28  27  26
    R2 [ 5                         25 ] T2
    R3 [ 6                         24 ] T3
    R4 [ 7                  ●      23 ] T4
    NC [ 8                         22 ] NC
    R5 [ 9                         21 ] T5
    R6 [ 10                        20 ] T6
    R7 [ 11                        19 ] T7
          12  13  14  15  16  17  18

        ERR  CLR  GND  NC  CLK  OET  Parity
```

11229-006A

Am29C853A

DIPs*

```
      ___
OER [ 1●    24 ] Vcc
 R0 [ 2     23 ] T0
 R1 [ 3     22 ] T1
 R2 [ 4     21 ] T2
 R3 [ 5     20 ] T3
 R4 [ 6     19 ] T4
 R5 [ 7     18 ] T5
 R6 [ 8     17 ] T6
 R7 [ 9     16 ] T7
ERR [ 10    15 ] Parity
CLR [ 11    14 ] OET
GND [ 12    13 ] EN
```

11229-007A

PLCC

```
         R1  R0  OER  NC  Vcc  T0  T1

          4   3   2   1   28  27  26
    R2 [ 5                         25 ] T2
    R3 [ 6                         24 ] T3
    R4 [ 7                  ●      23 ] T4
    NC [ 8                         22 ] NC
    R5 [ 9                         21 ] T5
    R6 [ 10                        20 ] T6
    R7 [ 11                        19 ] T7
          12  13  14  15  16  17  18

        ERR  CLR  GND  NC  EN  OET  Parity
```

11229-008A

*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

FUNCTION TABLES
Am29C833A (Register Option)

OET	OER	CLR	CLK	Ri	Sum of H's of Ri	Ti	Sum of H's (Ti + Parity)	Ri	Ti	Parity	ERR	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care or Irrelevant

Z = High Impedance
NA= Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN= Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

Am29C853A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i+ Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care or Irrelevant

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLES

Error Flag Output
Am29C833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	
H	↑	X	L	L	Sample (1's Capture)
H	↑	L	X	L	
L	X	X	X	H	Clear

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

Error Flag Output
Am29C853A

Inputs		Internal to Device	Outputs Pre-state	Output	
EN	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	
L	H	X	L	L	Sample (1's Capture)
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. **Device Number**
    b. **Speed Option (if applicable)**
    c. **Package Type**
    d. **Temperature Range**
    e. **Optional Processing**

AM29C833A
AM29C853A
                      P   C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-mil) Plastic DIP (PD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C833A
CMOS Parity Bus Transceiver – Register Option
Am29C853A
CMOS Parity Bus Transceiver – Latch Option

Valid Combinations	
AM29C833A	PC, SC, JC
AM29C853A	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

    a.   **Device Number**
    b.   **Speed Option (if applicable)**
    c.   **Device Class**
    d.   **Package Type**
    e.   **Lead Finish**

```
AM29C833A
AM29C853A                    /B   L   A
```

e. LEAD FINISH
    A = Hot Solder Dip

d. PACKAGE TYPE
    L = 24-Pin Slim Ceramic DIP (CD3024)

c. DEVICE CLASS
    /B = Class B

b. SPEED OPTION
    Not Applicable

a. DEVICE NUMBER/DESCRIPTION
    Am29C833A
    CMOS Parity Bus Transceiver – Register Option
    Am29C853A
    CMOS Parity Bus Transceiver – Latch Option

Valid Combinations	
AM29C833A	/BLA
AM29C853A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION
Am29C833A/Am29C853A
$\overline{\text{OER}}$
Output Enable Receive (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OET}}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{\text{OET}}$
Output Enable Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OER}}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i
Receive Port (Input/Output, Three-State)

R_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

T_i
Transmit Port (Input/Output, Three-State)

T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity
Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29C833A Only
$\overline{\text{ERR}}$
Error Flag (Output, Open Drain)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the register is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, the Error Flag Register is cleared ($\overline{\text{ERR}}$ goes HIGH).

CLK
Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

Am29C853A Only
$\overline{\text{ERR}}$
Error Flag (Output, Open Drain)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the latch is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, the Error Flag latch is cleared ($\overline{\text{ERR}}$ goes HIGH).

$\overline{\text{EN}}$
Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature $\quad\quad\quad$ −65 to +150°C

Supply Voltage to Ground
Potential Continuous $\quad\quad\quad$ −0.5 V to +7.0 V

DC Output Voltage $\quad\quad\quad$ −0.5 V to +6.0 V

DC Input Voltage $\quad\quad\quad$ −0.5 V to +6.0 V

DC Output Diode Current:
   Into Output $\quad\quad\quad$ +50 mA
   Out of Output $\quad\quad\quad$ −50 mA

DC Input Diode Current:
   Into Input $\quad\quad\quad$ +20 mA
   Out of Input $\quad\quad\quad$ −20 mA

DC Output Current per Pin:
   Into Output $\quad\quad\quad$ +100 mA
   Out of Output $\quad\quad\quad$ −100 mA

Total DC Ground Current
   $(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)

Total DC V_{CC} Current
   $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
   Ambient Temperature (T_A) $\quad\quad$ 0 to +70°C
   Supply Voltage (V_{CC}) $\quad\quad$ +4.5 to +5.5 V

Military (M) Devices
   Ambient Temperature (T_A) $\quad\quad$ −55 to +125°C
   Supply Voltage (V_{CC}) $\quad\quad$ +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified
(for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions				Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 4.5$ V, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15$ mA			2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = 4.5$ V, $V_{IN} = V_{IH}$ or V_{IL}	MIL $I_{OL} = 32$ mA				0.5	V
			COM'L $I_{OL} = 48$ mA				0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage (Note 1)	Am29C853A	All Inputs		2		V
			Am29C833A					
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)					0.8	V
V_I	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA					-1.2	V
I_{IL}	Input LOW Current	$V_{CC} = 5.5$ V, Input Only	$V_{IN} = 0.0$ V				-5	μA
I_{IH}	Input HIGH Current	$V_{CC} = 5.5$ V, Input Only	$V_{IN} = 5.5$ V				5	μA
I_{OZH}	Output Off-State Current	$V_{CC} = 5.5$ V, I/O Port	$V_{OUT} = 5.5$ V				10	μA
I_{OZL}	(High Impedance)	$V_{CC} = 5.5$ V, I/O Port	$V_{OUT} = 0.0$ V				-10	μA
I_{SC}	Output Short-Circuit Current	$V_{CC} = 5.5$ V, $V_O = 0$ V (Note 2)				-60		mA
I_{CCQ}	Static Supply Current	$V_{CC} = 5.5$ V Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL			1.5	mA
				COM'L			1.2	
I_{CCT}			$V_{IN} = 3.4$ V	R_i, T_i, Parity			1.5	mA/ Bit
				$\overline{CLR}$, CLK, (Note 4) $\overline{OET}$, $\overline{OER}$			3.0	
I_{CCD}†	Dynamic Supply Current	$V_{CC} = 5.5$ V (Note 3)	Outputs Open				275	μA/ MHz/ Bit
			Outputs Loaded				400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time, duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.
4. For Am29C853A, replace CLK with $\overline{EN}$.
† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description		Test Conditions*	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
tPLH	Propagation Delay to R_i to T_i,			2	10.5	2	12	ns
tPHL	T_i to R_i (Note 3)			2	10.5	2	12	ns
tPLH	Propagation Delay R_i to Parity			4	13	4	14.5	ns
tPHL				4	13	4	14.5	ns
tZH	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i			2	10.5	2	12	ns
tZL	and Parity			2	10.5	2	12	ns
tHZ	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i			1.5	10.5	1.5	12	ns
tLZ	and Parity			1.5	10.5	1.5	12	ns
ts	T_i, Parity to CLK Setup Time (Note 1)		$C_L = 50$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	8		10		ns
tH	T_i, Parity to CLK	Am29C833A		0		2		ns
	Hold Time (Note 1)	Am29C853A		1		3		ns
tREC	Clear ($\overline{CLR}\_\Gamma$) to CLK Setup Time (Note 2)			2		4		ns
tPWH	Clock Pulse Width (Note 1)	HIGH		6		9		ns
tPWL		LOW		6		9		ns
tPWL	Clear Pulse Width	LOW		6		9		ns
tPHL	Propagation Delay CLK to $\overline{ERR}$ (Note 1)			2	10	2	14	ns
tPLH	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$			8	18	8	21	ns
tPLH	Propagation Delay T_i, Parity to $\overline{ERR}$			6	19	6	21	ns
tPHL	(PASS Mode Only) Am29C853A			6	19	6	21	ns
tPLH	Propagation Delay $\overline{OER}$ to Parity			2	13	2	15	ns
tPHL				2	13	2	15	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For Am29C853A, replace CLK with $\overline{EN}$.

2. Applies only to Am29C833A.

3. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

Am29C833A/Am29C853A

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 4)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay to R_i to T_i,		2	14	2	15.5	ns
t_{PHL}	T_i to R_i (Note 3)		2	15	2	16.5	ns
t_{PLH}	Propagation Delay R_i to Parity		4	18	4	19.5	ns
t_{PHL}		$C_L = 300$ pF	4	18	4	19.5	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i	$R_1 = 500\ \Omega$	2	14	2	15.5	ns
t_{ZL}	and Parity	$R_2 = 500\ \Omega$	2	18.5	2	20.0	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity		2	18	2	20	ns
t_{PHL}			2	17	2	19	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i	$C_L = 5$ pF	1.5	7	1.5	8.5	ns
t_{LZ}	and Parity	$R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	1.5	7	1.5	8.5	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For Am29C853A, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833A.
3. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
4. These parameters are guaranteed by characterization but not production tested.

Am29C841A/Am29C843A
High Performance CMOS Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- **High-speed parallel latches**
  – D-Y propagation delay = 5 ns typical

- **Low standby power**

- **Very high output drive**
  – I_{OL} = 48 mA commercial, 32 mA Military

- **Extra-wide (9- and 10-bit) data paths**

- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**

- **Power-up/down disable circuit provides for glitch-free power supply sequencing**

- **Can be powered off while in 3-state, ideal for card edge interface applications**

- **Minimal speed degradation with multiple outputs switching**

- **200 mV typical hysteresis on data input path**

- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C841A and Am29C843A CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A latches are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C841A is a buffered, 10-bit version of the popular '373 function. The Am29C843A is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance micro–programmed systems.

The Am29C841A and Am29C843A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce) undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing

have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry which utilizes n-channel pull-up transistors (eliminating the parasitic diode to V_{CC}), provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C841A and Am29C843A are available in the standard package options: DIPs, PLCCs, and SOICs.

* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

BLOCK DIAGRAMS
Am29C841A

11230-001A

Am29C843A

11230-002A

CONNECTION DIAGRAMS
Top View
Am29C841A

DIPs*

$\overline{OE}$	1	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	LE

11230-003A

PLCC

Top pins: D_1 (4), D_0 (3), $\overline{OE}$ (2), NC (1), V_{CC} (28), Y_0 (27), Y_1 (26)

Left pins: D_2 (5), D_3 (6), D_4 (7), NC (8), D_5 (9), D_6 (10), D_7 (11)

Right pins: Y_2 (25), Y_3 (24), Y_4 (23), NC (22), Y_5 (21), Y_6 (20), Y_7 (19)

Bottom pins: D_8 (12), D_9 (13), GND (14), NC (15), LE (16), Y_9 (17), Y_8 (18)

11230-004A

Am29C843A

DIPs*

$\overline{OE}$	1	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
$\overline{CLR}$	11	14	$\overline{PRE}$
GND	12	13	LE

11230-005A

PLCC

Top pins: D_1 (4), D_0 (3), $\overline{OE}$ (2), NC (1), V_{CC} (28), Y_0 (27), Y_1 (26)

Left pins: D_2 (5), D_3 (6), D_4 (7), NC (8), D_5 (9), D_6 (10), D_7 (11)

Right pins: Y_2 (25), Y_3 (24), Y_4 (23), NC (22), Y_5 (21), Y_6 (20), Y_7 (19)

Bottom pins: D_8 (12), $\overline{CLR}$ (13), GND (14), NC (15), LE (16), $\overline{PRE}$ (17), Y_8 (18)

11230-006A

*Also available in 24-Pin Small Outline Package; pinout identical to DIPs.

Note:

Pin 1 is marked for orientation

LOGIC SYMBOLS

Am29C841A

11230-007A

Am29C843A

11230-008A

FUNCTION TABLES

Am29C841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843A

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = HIGH   NC = No Change
L = LOW   Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**

AM29C841A
AM29C843A   P   C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C841A CMOS 10-Bit Latch
Am29C843A CMOS 9-Bit Latch
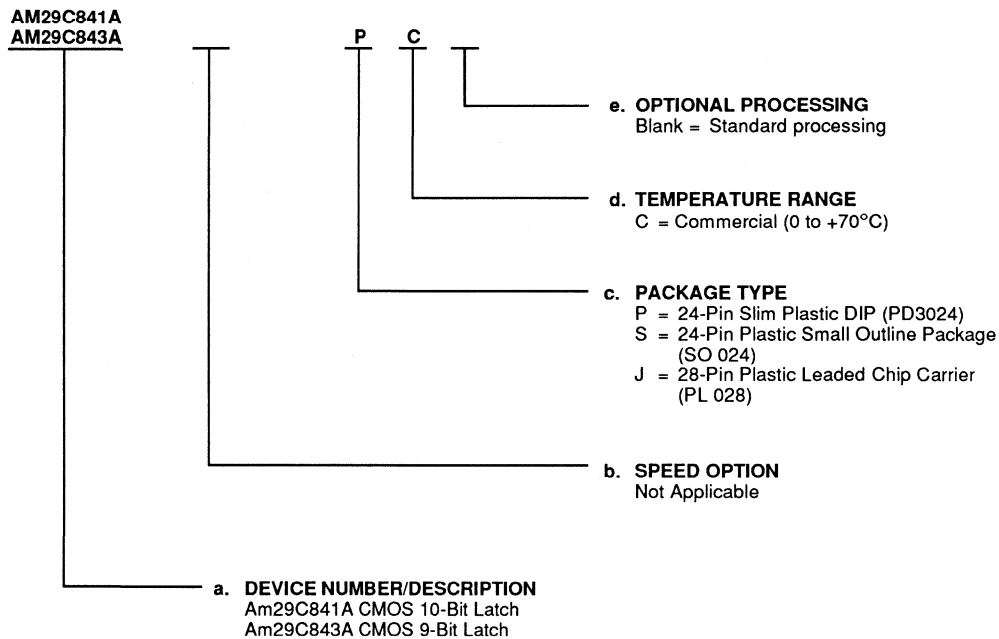
Valid Combinations	
AM29C841A	PC, SC, JC
AM29C843A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**

AM29C841A
AM29C843A ——— /B   L   A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C841A CMOS 10-Bit Latch
Am29C843A CMOS 9-Bit Latch

Valid Combinations	
AM29C841A	/BLA
AM29C843A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION
Am29C841A/Am29C843A

D_i

Data Inputs (Input)

D_i are the latch data inputs.

Y_i

Data Outputs (Output)

Y_i are the three state data outputs.

LE

Latch Enable (Input, Active HIGH)

The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$

Output Enable (Input, Active LOW)

When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedence state.

Am29C843A Only

$\overline{PRE}$

Preset (Input, Active LOW)

When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$

Clear (Input, Active LOW)

When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to $+150°C$

Supply Voltage to Ground
Potential Continuous -0.5 V to $+7$ V

DC Output Voltage -0.5 V to $+6$ V

DC Input Voltage -0.5 V to $+6$ V

DC Output Diode Current:
  Into Output $+50$ mA
  Out of Output -50 mA

DC Input Diode Current:
  Into Input $+20$ mA
  Out of Input -20 mA

DC Output Current per Pin:
  Into Output $+100$ mA
  Out of Output -100 mA

Total DC Ground
Current $(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)

Total DC V_{CC}
Current $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)   0 to $+70°C$
Supply Voltage (V_{CC}) $+4.5$ V to $+5.5$ V

Military (M) Devices

Ambient Temperature (T_A) -55 to $+125°C$
Supply Voltage (V_{CC}) $+4.5$ V to $+5.5$ V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V Min.	MIL I_{OL} = 32 mA			0.5	V
		V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} = 48 mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−5	μA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				5	μA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V				+10	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = GND				−10	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OE}$, $\overline{PRE}$ $\overline{CLR}$, LE		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)	Outputs Open			275	μA/ MHz/ Bit
			Outputs Loaded			400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.

2. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.

3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i			2	7.5	2	8.5	ns
t_{PHL}	(LE = HIGH) (Note 1)			2	7.5	2	8.5	ns
t_s	Data to LE Setup Time			2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i			1	8	1	9	ns
t_{PHL}				2	8	2	9	ns
t_{PLH}	Propagation Delay, Preset to Y_i			2	9	2	11	ns
t_{PHL}				2	9	2	11	ns
t_{REC}	Preset ($\overline{PRE}$ ⌐) to LE Setup Time		C_L = 50 pF	4		4		ns
t_{PLH}	Propagation Delay, Clear to Y_i		R_1 = 500 Ω	2	11	2	12	ns
t_{PHL}			R_2 = 500 Ω	2	11	2	12	ns
t_{REC}	Clear ($\overline{CLR}$ ⌐) to LE Setup Time			3		3		ns
t_{PWH}	LE Pulse Width	HIGH		4		4		ns
t_{PWL}	Preset Pulse Width	LOW		4		4		ns
t_{PWL}	Clear Pulse Width	LOW		4		4		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i			1	9	1	9.5	ns
t_{ZL}				3	12	3	13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i			2	8	2	8.5	ns
t_{LZ}				2	8	2	8.5	ns

*See Switching Test Circuit and Waveforms listed in Chapter 2.

Note:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (Chapter 3).

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description (Note 2)	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i	C_L = 300 pF R_1 = 500 Ω R_2 = 500 Ω	2	14.5	2	16.0	ns
t_{PHL}	(LE = HIGH) (Note 1)		2	14.5	2	16.0	ns
t_{PLH}	Latch Enable (LE) to Y_i		2	16.5	2	18	ns
t_{PHL}			2	16.5	2	18	ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		2	16.5	2	17.0	ns
t_{ZL}			3	19.5	3	20.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i	C_L = 5 pF R_1 = 500 Ω R_2 = 500 Ω	2	7	2	7.5	ns
t_{LZ}			2	7	2	7.5	ns

*See Switching Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (Chapter 3).

2. These parameters are guaranteed by characterization but not production tested.

Am29C861A/Am29C863A

High Performance CMOS Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS bidirectional bus transceivers**
  - T-R delay = 4 ns typical

- **Low standby power**

- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military

- **200-mV typical hysteresis on data input ports**

- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**

- **Power-up/down disable circuit provides for glitch-free power supply sequencing**

- **Can be powered off while in 3-state, ideal for card edge interface applications**

- **Minimal speed degradation with multiple outputs switching**

- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C861A and Am29C863A CMOS Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29C861A is a 10-bit bidirectional transceiver; the Am29C863A is a 9-bit transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C861A and Am29C863A are produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 4 ns, as well as an output current drive of 48 mA.

The Am29C861A and Am29C863A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have

been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry which utilizes n-channel pull-up transistors (eliminating the parasitic diode to V_{CC}) provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C861A and Am29C863A are available in the standard package options: DIPs, PLCCs, and SOICs.

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* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

BLOCK DIAGRAMS
Am29C861A
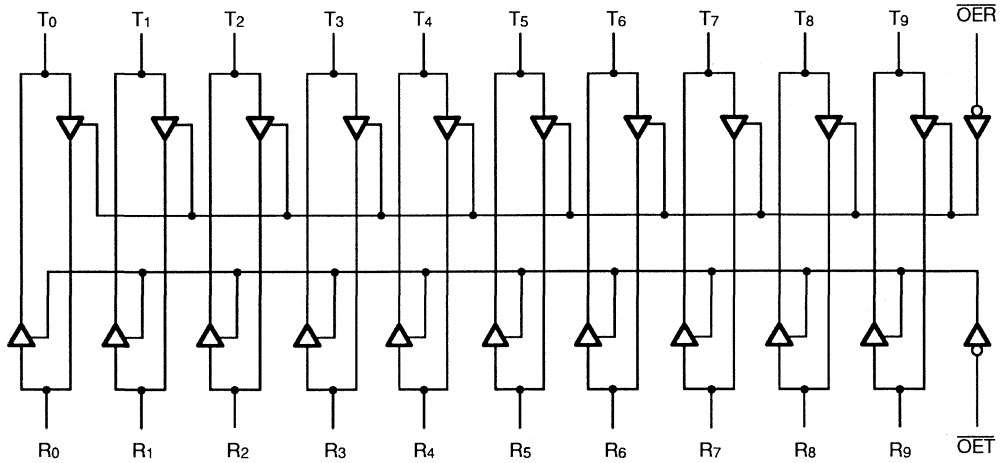
11231-001A

Am29C863A
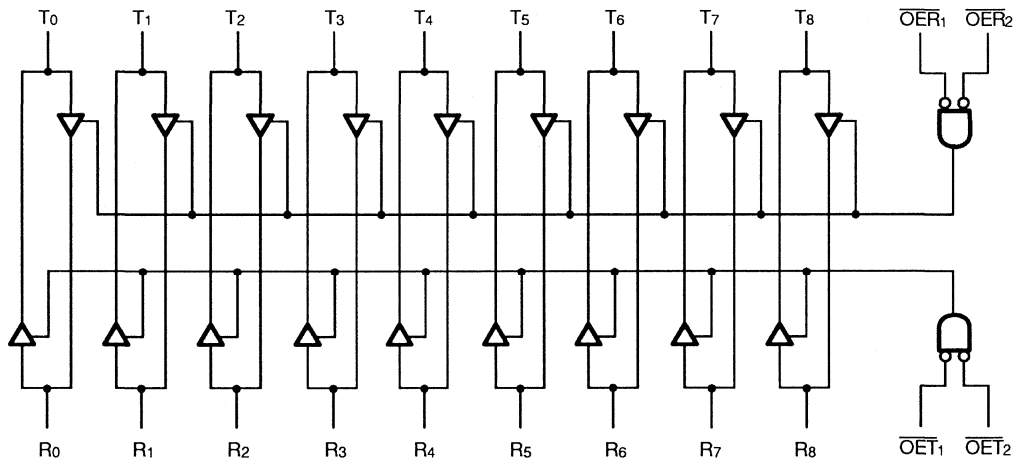
11231-002A

CONNECTION DIAGRAMS
Top View
Am29C861A

DIP*

$\overline{OER}$	1	24	V_{CC}
R_0	2	23	T_0
R_1	3	22	T_1
R_2	4	21	T_2
R_3	5	20	T_3
R_4	6	19	T_4
R_5	7	18	T_5
R_6	8	17	T_6
R_7	9	16	T_7
R_8	10	15	T_8
R_9	11	14	T_9
GND	12	13	$\overline{OET}$

11231-003A

PLCC

Top: R_1(4), R_0(3), $\overline{OER}$(2), NC(1), V_{CC}(28), T_0(27), T_1(26)

Left: R_2(5), R_3(6), R_4(7), NC(8), R_5(9), R_6(10), R_7(11)

Bottom: R_8(12), R_9(13), GND(14), NC(15), $\overline{OET}$(16), T_9(17), T_8(18)

Right: T_2(25), T_3(24), T_4(23), NC(22), T_5(21), T_6(20), T_7(19)
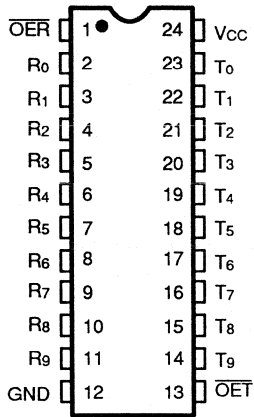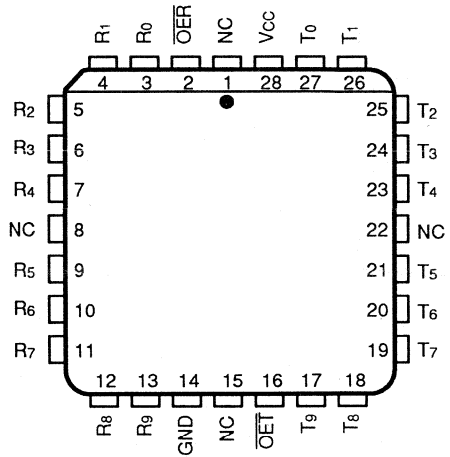
11231-004A

Am29C863A

DIP*

$\overline{OER}_1$	1	24	V_{CC}
R_0	2	23	T_0
R_1	3	22	T_1
R_2	4	21	T_2
R_3	5	20	T_3
R_4	6	19	T_4
R_5	7	18	T_5
R_6	8	17	T_6
R_7	9	16	T_7
R_8	10	15	T_8
$\overline{OER}_2$	11	14	$\overline{OET}_2$
GND	12	13	$\overline{OET}_1$

11231-005A

PLCC

Top: R_1(4), R_0(3), $\overline{OER}_1$(2), NC(1), V_{CC}(28), T_0(27), T_1(26)

Left: R_2(5), R_3(6), R_4(7), NC(8), R_5(9), R_6(10), R_7(11)

Bottom: R_8(12), $\overline{OER}_2$(13), GND(14), NC(15), $\overline{OET}_1$(16), $\overline{OET}_2$(17), T_8(18)

Right: T_2(25), T_3(24), T_4(23), NC(22), T_5(21), T_6(20), T_7(19)
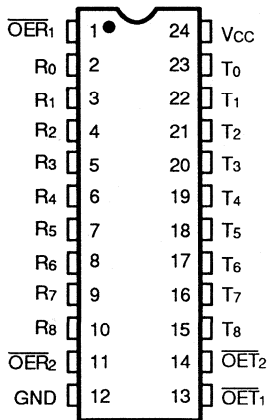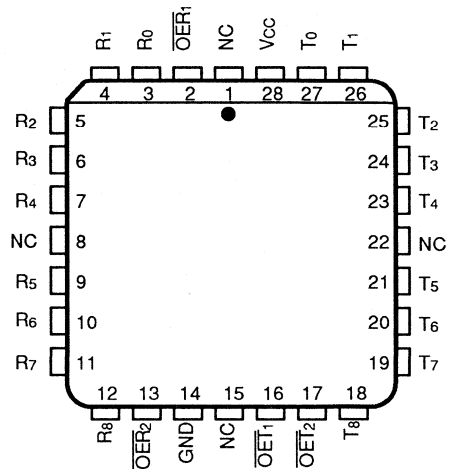
11231-006A

*Also available in 24-Pin Small Outline Package; pinout identical to DIPs.

Note:

Pin 1 is marked for orientation

LOGIC SYMBOLS

Am29C861A
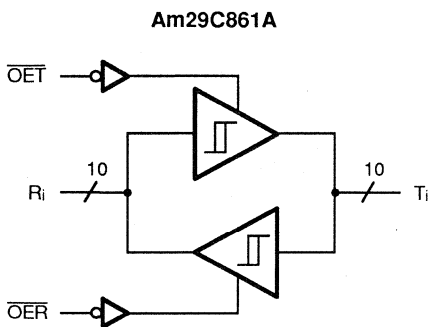
11231-007A
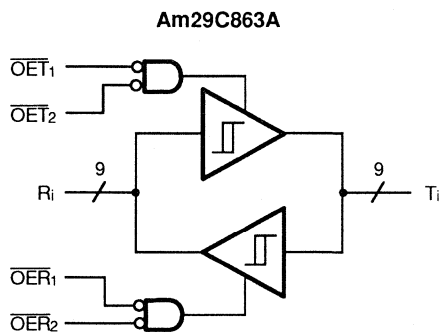
Am29C863A

11231-008A

FUNCTION TABLES

Am29C861A

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29C863A

Inputs						Outputs		
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_i	T_i	R_i	T_i	Function
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH   NC = Not Applicable
L = LOW   Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**

AM29C861A
AM29C863A   P   C

e. **OPTIONAL PROCESSING**
Blank = Standard processing

d. **TEMPERATURE RANGE**
C = Commercial (0 to +70°C)

c. **PACKAGE TYPE**
P = 24-Pin Slim Plastic DIP (PD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. **SPEED OPTION**
Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**
Am29C861A CMOS 10-Bit Transceiver
Am29C863A CMOS 9-Bit Transceiver
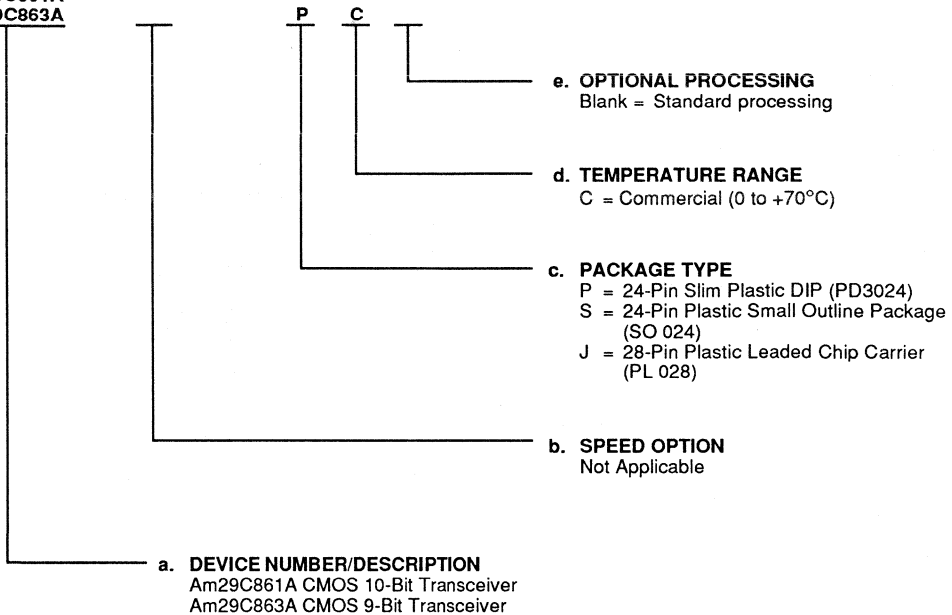
Valid Combinations	
AM29C861A	PC, SC, JC
AM29C863A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

    a.   **Device Number**
    b.   **Speed Option (if applicable)**
    c.   **Device Class**
    d.   **Package Type**
    e.   **Lead Finish**

```
AM29C861A
AM29C863A          /B    L    A
```

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C861A CMOS 10-Bit Transceiver
Am29C863A CMOS 9-Bit Transceiver

Valid Combinations	
AM29C861A	/BLA
AM29C863A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION
Am29C861A Only
$\overline{OER}$
Output Enable Receive (Input, Active Low)

When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$
Output Enable Transmit (Input, Active Low)

When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_i
Receive Port (Input/Output)

R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output)

T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29C863A Only
$\overline{OER}_i$
Output Enables Receive (Input, Active Low)

When both $\overline{OER}_1$ and $\overline{OER}_2$ are LOW while $\overline{OET}_1$ or $\overline{OET}_2$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}_i$
Output Enables Transmit (Input, Active Low)

When both $\overline{OET}_1$ and $\overline{OET}_2$ are LOW while $\overline{OER}_1$ or $\overline{OER}_2$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_i
Receive Port (Input/Output)

R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output)

T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Output Voltage	−0.5 V to +6.0 V
DC Input Voltage	−0.5 V to +6.0 V

DC Output Diode Current: Into Output   + 50 mA
                          Out of Output − 50 mA

DC Input Diode Current: Into Input   + 20 mA
                          Out of Input   − 20 mA

DC Output Current: Into Output   + 100 mA
                          Out of Output − 100 mA

Total DC Ground Current (n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA			0.5	V
			COM'L, I_{OL} = 48 mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0 V			−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 5.5 V			5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 5.5 V			10	µA
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0 V			−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OER}_1$, $\overline{OER}_2$ $\overline{OET}_1$, $\overline{OET}_2$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)	Outputs Open			275	µA/
			Outputs Loaded			400	MHz/ Bit

Notes:

1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.
† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Am29C861A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	7	2	8	ns
t_{PHL}			2	8	2	9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	10	2	11	ns
t_{ZL}			2	12.5	2	13.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		1.5	9	1.5	10	ns
t_{LZ}			1.5	10	1.5	11	ns

Am29C863A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	7	2	8	ns
t_{PHL}			2	8	2	9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	10.5	2	11.5	ns
t_{ZL}			2	12.5	2	13.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		1.5	10	1.5	11	ns
t_{LZ}			1.5	11	1.5	12	ns

* See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 2)

Am29C861A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	$C_L = 300$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	2	14.5	2	15.5	ns
t_{PHL}			2	15.5	2	16.5	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	16.5	2	17.5	ns
t_{ZL}			2	20.5	2	21.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	$C_L = 5$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	1.5	7	1.5	8	ns
t_{LZ}			1.5	8.5	1.5	9.5	ns

Am29C863A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	$C_L = 300$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	2	14.5	2	15.5	ns
t_{PHL}			2	15.5	2	16.5	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	16.5	2	17.5	ns
t_{ZL}			2	20.5	2	21.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	$C_L = 5$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	1.5	7	1.5	8	ns
t_{LZ}			1.5	8.5	1.5	9.5	ns

* See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

2. These parameters are guaranteed by characterization but not production tested.

CHAPTER 5
Bipolar Family Data Sheets

Am29818A

Pipeline Register with SSR™ Diagnostics

DISTINCTIVE CHARACTERISTICS

- **High-speed noninverting 8-bit parallel register for any data path or pipelining application**
- **WCS (Writable Control Store) pipeline register**
  - Load WCS from serial register
  - Read WCS via serial scan
- **Alternate sourced as SN54/74S818**

- **High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics**
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- **Speed comparable with that of 'AS374 register**

GENERAL DESCRIPTION

The Am29818A is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a shift register. In the se-

rial shift mode, SDI is shifted into the '0' location of the Shadow register and the contents of '7' location appear at the SDO output. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29818A Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM

08611-001A

CONNECTION DIAGRAM
Top View

DIP

```
          ┌───┐  ┌───┐
  OEY ──┤ 1 ●    24 ├── Vcc
 DCLK ──┤ 2      23 ├── MODE
   D0 ──┤ 3      22 ├── Y0
   D1 ──┤ 4      21 ├── Y1
   D2 ──┤ 5      20 ├── Y2
   D3 ──┤ 6      19 ├── Y3
   D4 ──┤ 7      18 ├── Y4
   D5 ──┤ 8      17 ├── Y5
   D6 ──┤ 9      16 ├── Y6
   D7 ──┤ 10     15 ├── Y7
  SDI ──┤ 11     14 ├── SDO
  GND ──┤ 12     13 ├── PCLK
          └─────────┘
```

08611-002A

Am29818A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. **Device Number**
    b. **Speed Option (if applicable)**
    c. **Package Type**
    d. **Temperature Range**
    e. **Optional Processing**

AM29818A   **P**   **C**

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29818A
Pipeline Register with SSR Diagnostics

Valid Combinations	
AM29818A	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$D_0 - D_7$
Parallel Data Inputs (Input/Output)

Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK
Diagnostics Clock (Input)

Diagnostics/WCS clock for loading shadow register (serial or parallel modes – see Function Table).

MODE
Mode Control (Input)

Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$
Y-Port Output Enable (Input: Active LOW)

Active LOW output enable for Y-port.

PCLK
Pipeline Register Clock (Input)

Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI
Serial Data Input (Input)

Input to shadow register (see Function Table).

SDO
Serial Data Output (Output)

Output from shadow register.

$Y_0 - Y_7$
Parallel Data Outputs (Input/Output)

Data outputs from the pipeline register and parallel inputs to the shadow register.

FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no setup or hold times are violated, this simultaneous operation is legal.

FUNCTION TABLE

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_0 \leftarrow SDI$	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	SDI	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Reg.
H	H	↑	X	SDI	Hold*	NA	Hold Shadow Register; $D_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

Table Definitions

Inputs

H = HIGH

L = LOW

X = Don't Care

↑ = LOW-to-HIGH Transition

Outputs

$S_7 - S_0$ = Shadow Register outputs

$P_7 - P_0$ = Pipeline Register outputs

$D_7 - D_0$ = Data I/O port

$Y_7 - Y_0$ = Y I/O port

NA = Not applicable, output is not a function of the specified input combinations.

SHADOW REGISTER
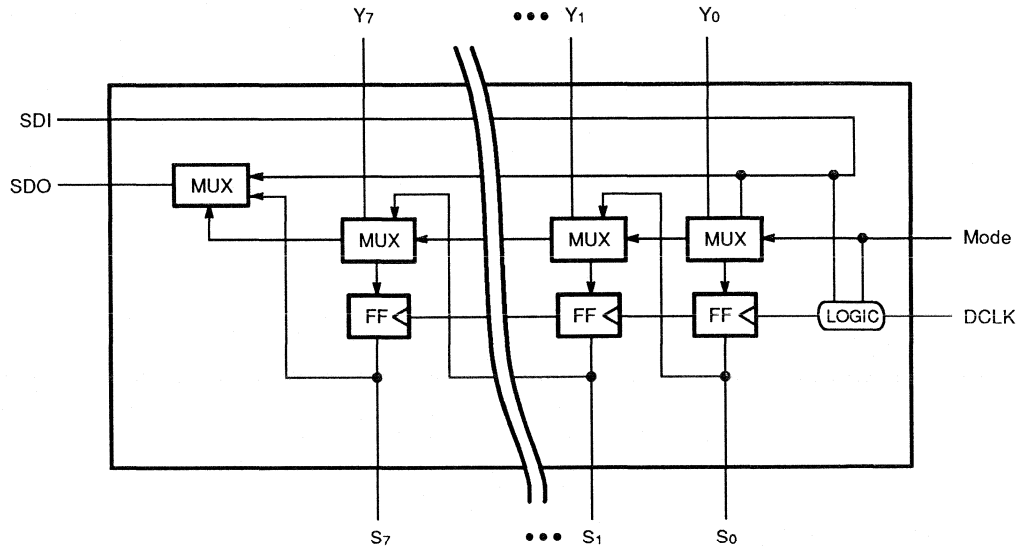
08611-005A

An Introduction to Serial Shadow Register (SSR) Diagnostics

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both observe intermediate test points and control intermediate signals – address, data, control and status – to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinatorial and Sequential Networks

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.

08611-006A

Figure 1. Combinatorial Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

08611-007A

Figure 2. Sequential Network

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinatorial network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.
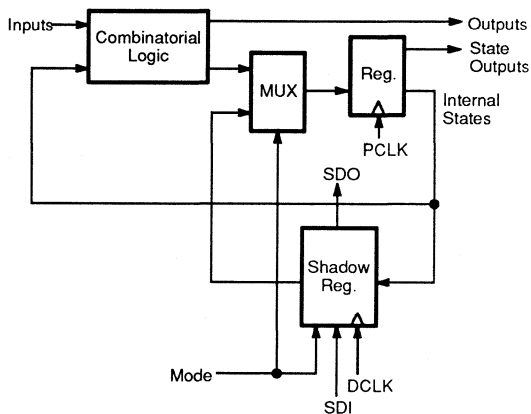
08611-008A

Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with

PCLK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinatorial networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

08611-009A

Figure 4. SSR Diagnostics Logical Path

A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29818A.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feedback paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818As can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.
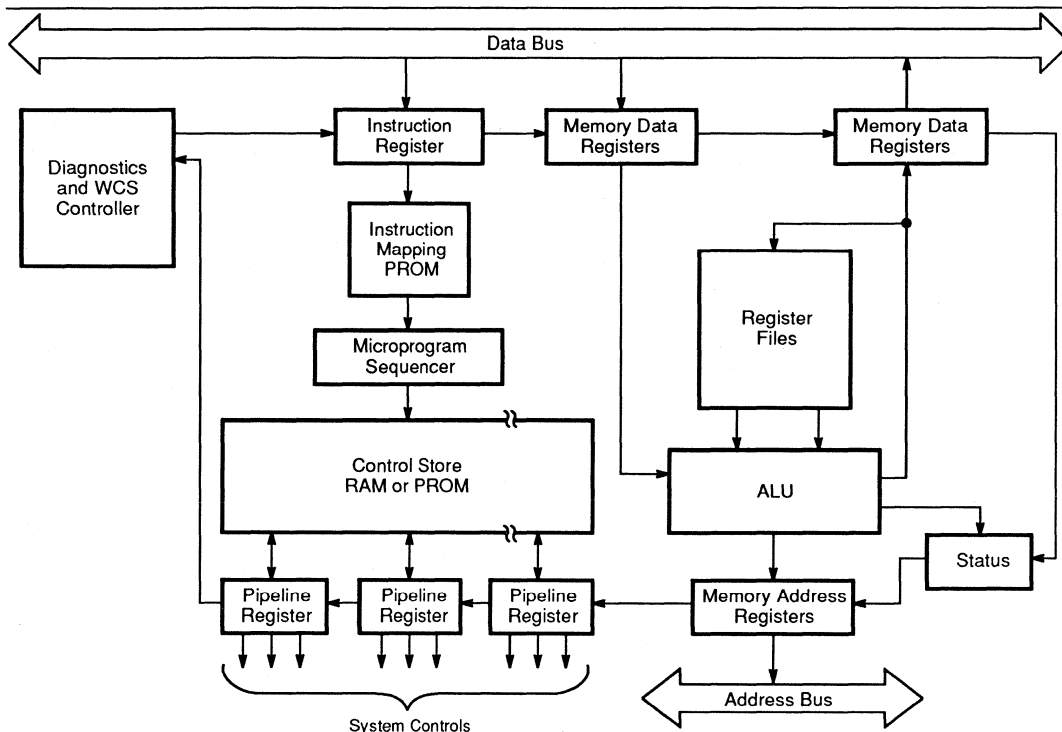
SSR Diagnostics/WCS Pipeline Registers
Replace Normal Registers with Diagnostics Loop

08611-010A

Figure 5. Typical System Configuration

Use of the Am29818A Pipeline Register in Writable Control Store (WCS) Designs

The Am29818A SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29818A supports all of the above operations (and more) without any support circuitry. Figure 6 shows

a typical WCS design with the Am29818A. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinatorial network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.
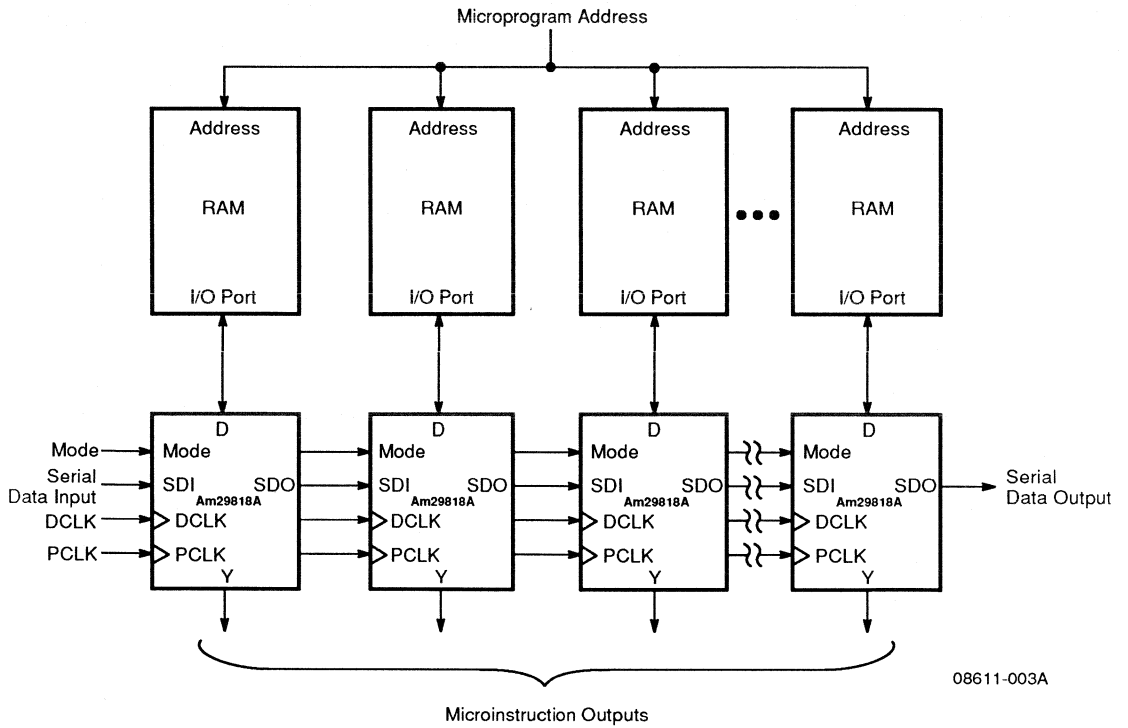
Figure 6. Am29818A-Based WCS Application

Figure 7. WCS Application without Am29818As

08611-004A

Am29818A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−1.5 V to +6.0 V
DC Output Current, into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V	$Y_0 - Y_7$	I_{OH} = −6 mA	2.4		V
		V_{IN} = V_{IH} or V_{IL}	$D_0 - D_7$, SDO	I_{OH} = −1 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V	$Y_0 - Y_7$	I_{OL} = 24 mA		0.5	V
		V_{IN} = V_{IH} or V_{IL}	$D_0 - D_7$, SDO	I_{OL} = 8 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.5 V				−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.4 V				50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} 5.5 V				100	μA
I_{OZ}	Off-State Current	V_{CC} = 5.5 V	V_O = 0.5 V			−250	μA
	(High-Impedance)		V_O = 2.4 V			100	
I_{SC}	Output Short-Circuit	V_{CC} = 5.5 V	$Y_0 - Y_7$		−30	−100	mA
	Current	(Note 2)	$D_0 - D_7$, SDO		−15	−50	
I_{OFF}	Bus Leakage	V_{CC} = 0 V, V_{OUT} = 2.9 V				100	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5 V	Outputs Hi-Z			145	mA

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.

2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t_{PLH} & t_{PHL}	PCLK → Yx			9	ns
	MODE → SDO			16	ns
	SDI → SDO			15	ns
	DCLK → SDO			25	ns
t_S	Dx → PCLK		4		ns
	MODE → PCLK		15		ns
	Yx → DCLK		5		ns
	MODE → DCLK		12		ns
	SDI → DCLK		10		ns
	DCLK → PCLK		15		ns
	PCLK → DCLK		40		ns
t_H	Dx → PCLK		2		ns
	MODE → PCLK		0		ns
	Yx → DCLK	$C_L = 50$ pF	5		ns
	MODE → DCLK		2		ns
	SDI → DCLK		0		ns
t_{LZ}	$\overline{OEY}$ → Yx			15	ns
	DCLK → Dx			45	ns
t_{HZ}	$\overline{OEY}$ → Yx			25	ns
	DCLK → Dx			80	ns
t_{ZL}	$\overline{OEY}$ → Yx			15	ns
	DCLK → Dx			25	ns
t_{ZH}	$\overline{OEY}$ → Yx			15	ns
	DCLK → Dx			25	ns
t_{PW}	PCLK (HIGH and LOW)		10		ns
	DCLK (HIGH and LOW)		15		ns

*See Test Circuit and Waveforms (Chapter 2).

Am29821/823/825

High Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
  - Noninverting CP-Y t_{PD} = 7.5 ns typ
  - Inverting CP-Y t_{PD} = 7.5 ns typ
- **Buffered common Clock Enable ($\overline{EN}$)**
- **Buffered common asynchronous Clear input ($\overline{CLR}$)**
- **Three-state outputs glitch free during power-up and down**
- **Outputs have Schottky clamp to ground**

- **48 mA Commercial I_{OL}**
- **Low input/output capacitance**
  - 6 pF inputs (typical)
  - 8 pF outputs (typical)
- **Metastable "Hardened" Registers**
- **I_{OH} specified at 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **IMOX™ high performance IMplanted OXide isolated process**

GENERAL DESCRIPTION

The Am29821/823/825 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 is a buffered, 10-bit wide version of the popular '374/'534 functions. The Am29823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 is an 8-bit buffered register with all the '823 controls plus mul-

tiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. It is ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAMS
Am29821
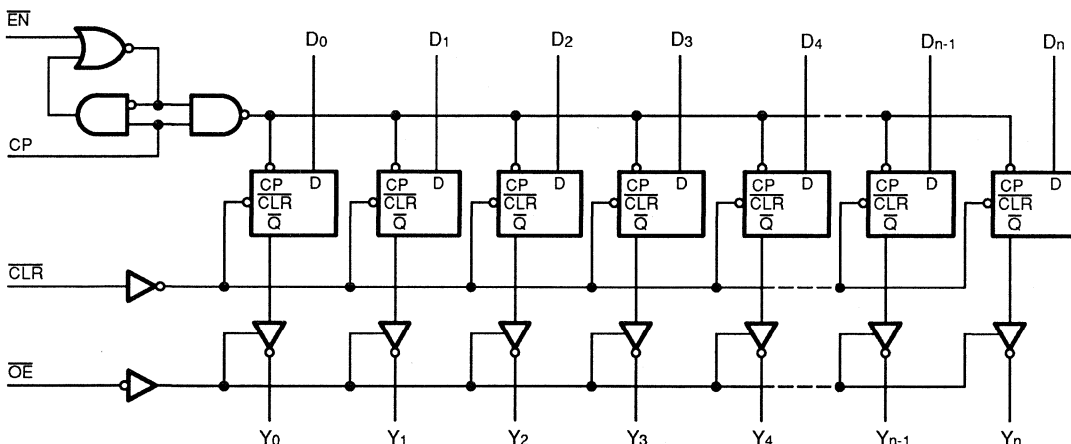
01420-001A

BLOCK DIAGRAMS (Continued)
Am29823
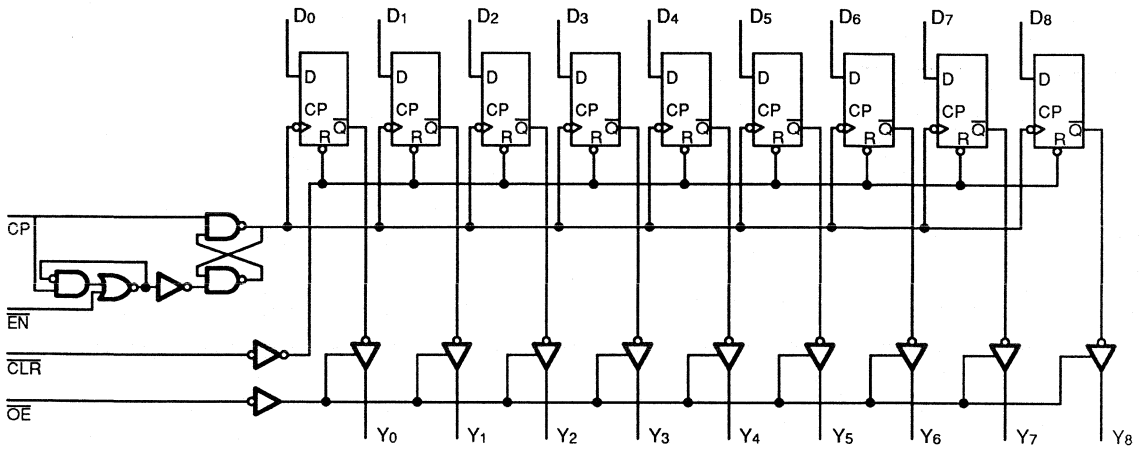
01420-002A

Am29825
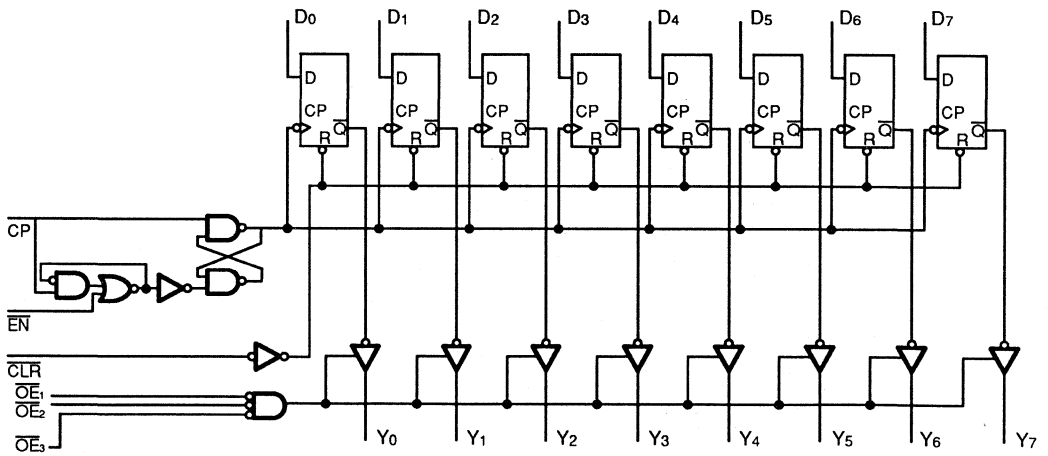
01420-003A

CONNECTION DIAGRAMS
Top View

Am29821

DIP

$\overline{OE}_1$	1	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	CP

01420-004A

Am29823

DIP

$\overline{OE}_1$	1	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
$\overline{CLR}$	11	14	$\overline{EN}$
GND	12	13	CP

01420-005A

Am29825

DIP
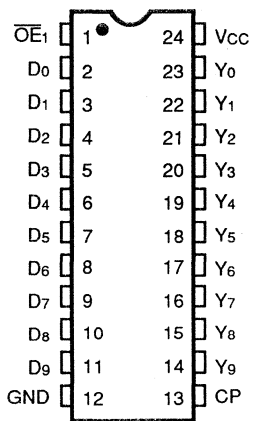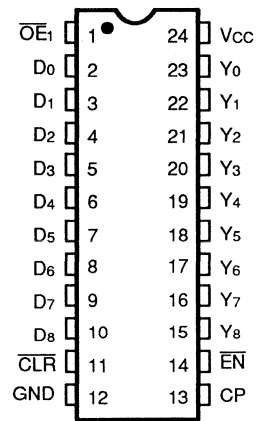
$\overline{OE}_1$	1	24	V_{CC}
$\overline{OE}_2$	2	23	$\overline{OE}_3$
D_0	3	22	Y_0
D_1	4	21	Y_1
D_2	5	20	Y_2
D_3	6	19	Y_3
D_4	7	18	Y_4
D_5	8	17	Y_5
D_6	9	16	Y_6
D_7	10	15	Y_7
$\overline{CLR}$	11	14	$\overline{EN}$
GND	12	13	CP
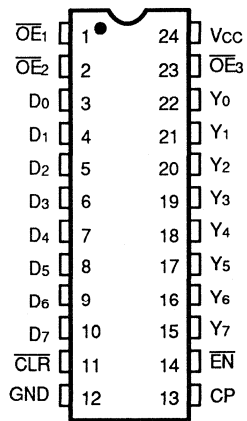
01420-006A

LOGIC SYMBOLS

Am29821
10-Bit Register
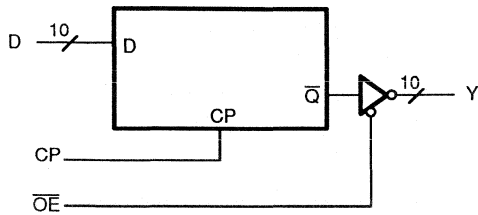
01420-007A

Am29823
9-Bit Register
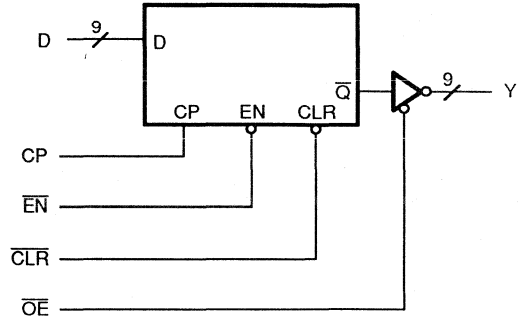
01420-008A

Am29825
8-Bit Register
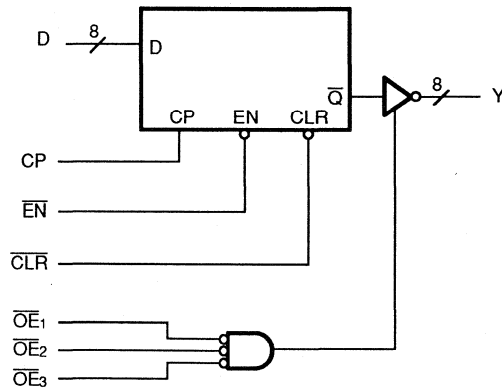
01420-009A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29821
AM29823
AM29825   P   C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29821
10-Bit Bus Interface Register

Am29823
9-Bit Bus Interface Register

Am29825
8-Bit Bus Interface Register
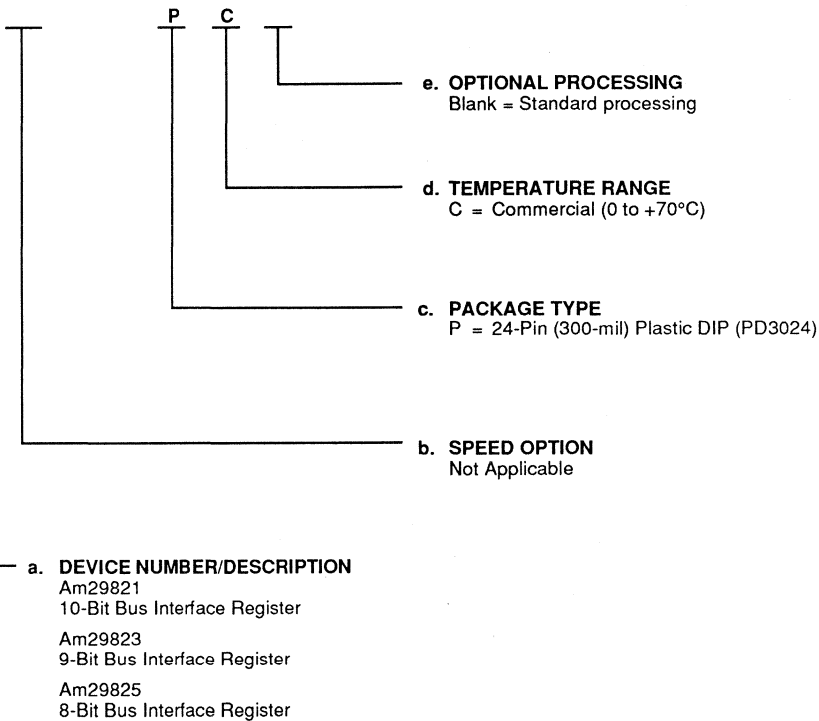
Valid Combinations	
AM29821	
AM29823	PC
AM29825	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

D_i

The D flip-flop data inputs.

$\overline{CLR}$

For both inverting and noninverting register, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.

CP

Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i

The register three-state outputs.

$\overline{EN}$

Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. (Note 1.)

$\overline{OE}$

Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

Note:

1. The Am29823 and Am29825 registers achieve short throughput delay and setup time and reduced power consumption by means of a clock gating and latching circuit. This circuit is sensitive to very short (<3 ns) HIGH-to-LOW-to-HIGH going spikes on $\overline{EN}$ while CP is HIGH. The designer should be aware of this and avoid the use of decoders or other potentially glitching devices in the $\overline{EN}$ logic.

FUNCTION TABLE

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	Function
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Ambient Temperature, (T_A)	0°C to +70°C
Supply Voltage, (V_{CC})	5.0 V ± 10%
	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V	Data, $\overline{CLR}$		−1.0	mA
			$\overline{OE}$, $\overline{EN}$, CP		−2.0	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			1.0	mA
I_{OZ}	Output Off-State (Hi-Z) Output Current	V_{CC} = 5.5 V	V_O = 0.4 V		−50	µA
			V_O = 2.4 V		50	
I_{SC}	Output Short Circuit Current (Note 1)	V_{CC} = 5.5 V		−75	−250	mA
I_{CC}	Supply Current (Note 2)	V_{CC} = 5.5 V Outputs Open $\overline{EN}$ = LOW	Over Temperature Range		140	mA
			+70°C		130	mA

Notes:
1. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
2. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		$C_L = 50$ pF	3.5		8.5	ns
t_{PHL}				3.5		10.5	ns
t_{PLH}			$C_L = 300$ pF			14	ns
t_{PHL}						18	ns
t_S	Data to CP Setup Time			2.0	0		ns
t_H	Data to CP Hold Time			2.0	0.5		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time			3.0	1.5		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time		$C_L = 50$ pF	3.0	1.5		ns
t_H	Enable ($\overline{EN}$) Hold Time			0	−1.5		ns
t_{PHL}	Propagation Delay, Clear to Y_i				12.9	15.0	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time			5.0	1.1		ns
t_{PWH}	Clock Pulse Width	HIGH		5.0	3.5		ns
t_{PWL}		LOW	$C_L = 50$ pF	5.0	3.0		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			5.0	4.0		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		$C_L = 300$ pF			17	ns
t_{ZL}						21	ns
t_{ZH}			$C_L = 50$ pF		11.5	12	ns
t_{ZL}					11.0	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i		$C_L = 50$ pF			9	ns
t_{LZ}						9	ns
t_{HZ}			$C_L = 5$ pF		5.2	8	ns
t_{LZ}					5.5	8	ns

Note:

1. See test circuit and waveforms (Chapter 2).

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Max.	Unit
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50 pF	3.5	10	ns
t_{PHL}				3.5	12	ns
t_{PLH}			C_L = 300 pF		16	ns
t_{PHL}					20	ns
t_S	Data to CP Setup Time			4		ns
t_H	Data to CP Hold Time			2		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time			4		ns
t_S	Enable ($\overline{EN}$ ⌐) to CP Setup Time			4		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		ns
t_{PHL}	Propagation Delay, Clear to Y_i		C_L = 50 pF		20	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time			7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		ns
t_{PWL}		LOW		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		C_L = 300 pF		20	ns
t_{ZL}					23	ns
t_{ZH}			C_L = 50 pF		14	ns
t_{ZL}					14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i		C_L = 50 pF		16	ns
t_{LZ}					12	ns
t_{HZ}			C_L = 5 pF		9	ns
t_{LZ}					9	ns

Note:

1. See test circuit and waveforms (Chapter 2).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

01420-010A

Am29827/Am29828

High Performance Buffers

DISTINCTIVE CHARACTERISTICS

- **High-speed buffers and inverters**
  - Noninverting t_{PD} = 5.0 ns typ
  - Inverting t_{PD} = 4.5 ns typ
- **200 mV minimum input hysteresis on input data ports**
- **Three-state outputs glitch-free during power-up and -down**
- **Outputs have Schottky clamp to ground**

- **48 mA commercial I_{OL}**
- **High capacitance load capability**
- **Low capacitance inputs and outputs**
- **I_{OH} specified 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **Fully TTL compatible inputs and outputs**
- **IMOX™ high performance IMplanted OXide isolated process**

GENERAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200 mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAMS
Am29827
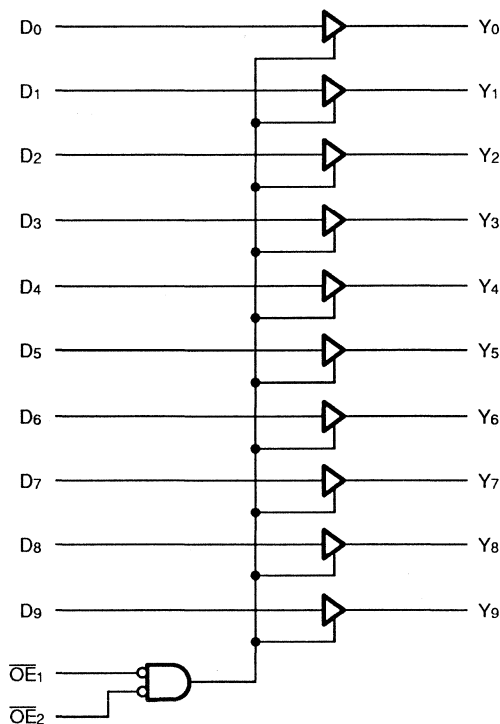
03371-001A

BLOCK DIAGRAMS (Continued)
Am29828

D_0 — ▷ — Y_0

D_1 — ▷ — Y_1

D_2 — ▷ — Y_2

D_3 — ▷ — Y_3

D_4 — ▷ — Y_4

D_5 — ▷ — Y_5

D_6 — ▷ — Y_6

D_7 — ▷ — Y_7

D_8 — ▷ — Y_8

D_9 — ▷ — Y_9

$\overline{OE}_1$

$\overline{OE}_2$
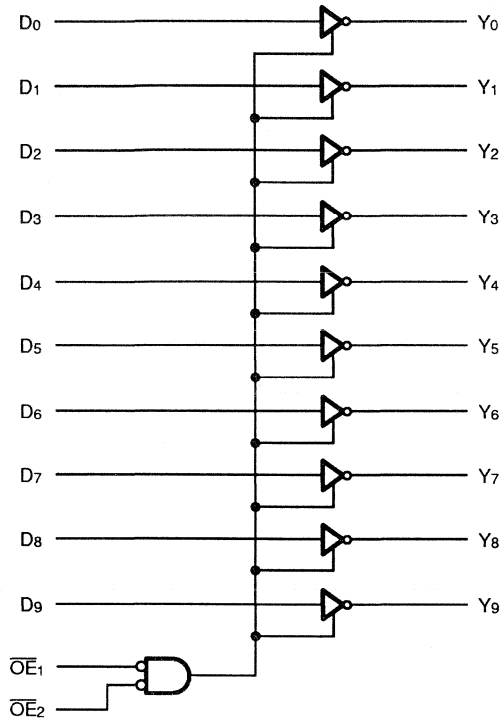
03371-002A

CONNECTION DIAGRAM

DIP

$\overline{OE}_1$	1	24	V_{CC}
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	$\overline{OE}_2$
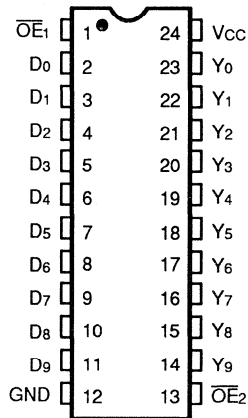
03371-003A

LOGIC SYMBOLS
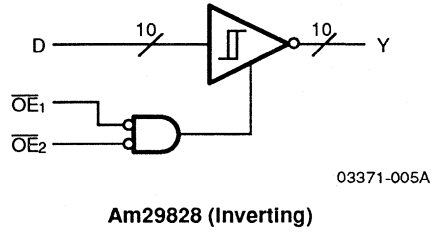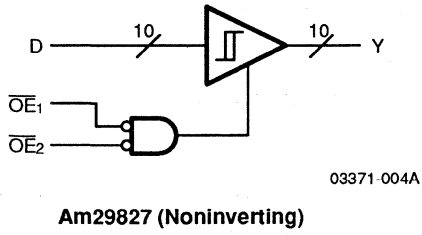
03371-004A

Am29827 (Noninverting)

03371-005A

Am29828 (Inverting)

Am29827/Am29828

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29827
AM29828   P   C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29827
10-Bit Noninverting Bus Buffer

Am29828
10-Bit Inverting Bus Buffer
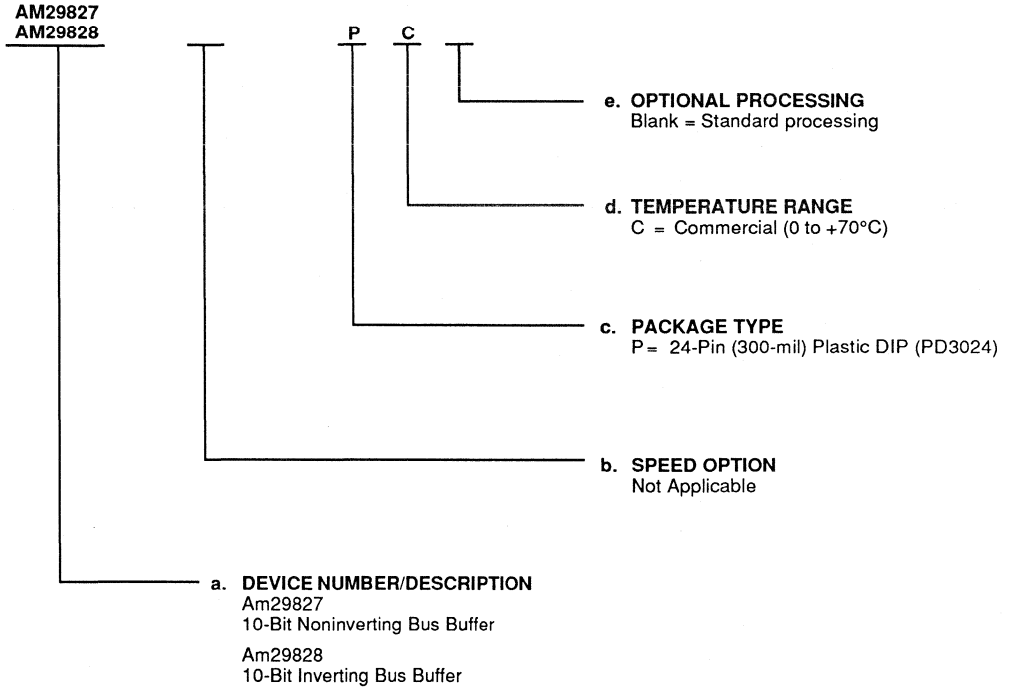
Valid Combinations	
AM29827	PC
AM29828	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{OE}_i$

When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are HI-Z.

D_i

10-bit data input.

Y_i

10-bit data output.

FUNCTION TABLES
Am29827 (Noninverting)

Inputs		Outputs	
$\overline{OE}$	D_i	Y_i	**Function**
L	H	H	Transparent
L	L	L	Transparent
H	X	Z	HI-Z

Am29828 (Inverting)

Inputs		Outputs	
$\overline{OE}$	D_i	Y_i	**Function**
L	H	L	Transparent
L	L	H	Transparent
H	X	Z	HI-Z

H	=	HIGH
L	=	LOW
X	=	Don't Care
Z	=	High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Output for High Output State	−1.5 V to +5.5 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Ambient Temperature, (T_A)	0°C to +70°C
Supply Voltage, (V_{CC})	5.0 V ± 10%
	4.5 V to 5.5 V

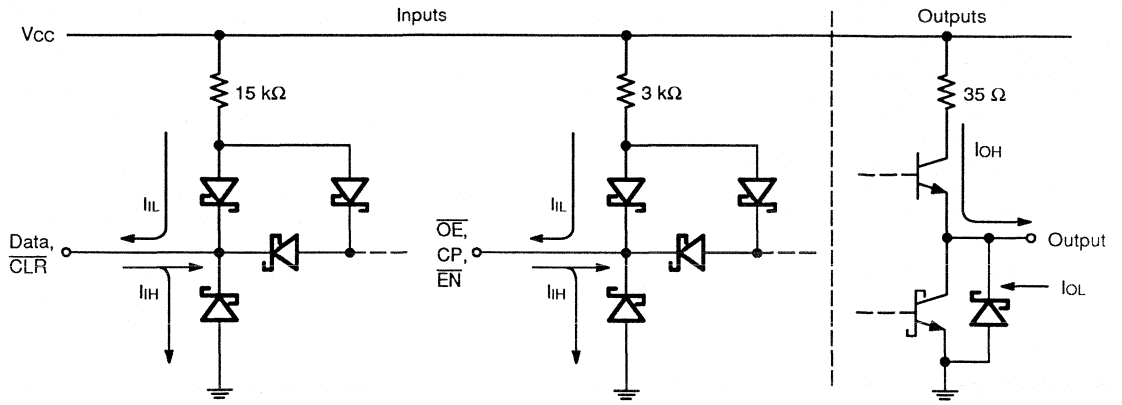*Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 4.5$ V	$I_{OH} = -15$ mA	2.4		V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24$ mA	2.0		V
V_{OL}	Output LOW Voltage	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA		0.5	V
		$V_{IN} = V_{IH}$ or V_{IL}				
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA			−1.2	V
V_{HYST}	Input Hysteresis	Output under test connected to AC load test circuit		200		mV
I_{IL}	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V			−1.0	mA
I_{IH}	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V			50	μA
I_I	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V			1.0	mA
I_{OZH}	Output Off-State Output Current (HI-Z)	$V_{CC} = 5.5$ V, $V_O = 2.4$ V			50	μA
I_{OZL}	Output Off-State Output Current (HI-Z)	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			−50	μA
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.5$ V		−75	−250	mA
I_{CC}	Supply Current	$V_{CC} = 5.5$ V	Over Temperature Range		80	mA
		Outputs Open	+70°C		75	

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Typ.	Max.	Unit
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	$C_L = 50$ pF		4.8	6.0	ns
t_{PHL}				5.2	6.2	ns
t_{PLH}		$C_L = 300$ pF		8.0	11	ns
t_{PHL}				10.8	13.2	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	$C_L = 50$ pF		4.0	5.2	ns
t_{PHL}				4.9	5.9	ns
t_{PLH}		$C_L = 300$ pF		7.3	10	ns
t_{PHL}				10.5	12.9	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	$C_L = 50$ pF		6.5	12	ns
t_{ZL}				9.5	12	ns
t_{ZH}		$C_L = 300$ pF		11	17	ns
t_{ZL}				18	21	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	$C_L = 5$ pF		3.5	8.0	ns
t_{LZ}				3.5	8.0	ns
t_{HZ}		$C_L = 50$ pF		11.2	16	ns
t_{LZ}				4.5	11	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	$C_L = 50$ pF		8	ns
t_{PHL}				8	ns
t_{PLH}		$C_L = 300$ pF		15	ns
t_{PHL}				15	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	$C_L = 50$ pF		7.0	ns
t_{PHL}				7.5	ns
t_{PLH}		$C_L = 300$ pF		14	ns
t_{PHL}				14	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	$C_L = 50$ pF		15	ns
t_{ZL}				15	ns
t_{ZH}		$C_L = 300$ pF		20	ns
t_{ZL}				23	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	$C_L = 5$ pF		9	ns
t_{LZ}				9	ns
t_{HZ}		$C_L = 50$ pF		17	ns
t_{LZ}				12	ns

*See Test Circuit and Waveforms (Chapter 2).

Am29827A

High-Performance Buffer

DISTINCTIVE CHARACTERISTICS

- **High speed buffers and inverters**
  - t_{PD} = 5.0 ns typ
  - Inverting t_{PD} = 4.5 ns typ
- **200 mV minimum input hysteresis on input data ports**

- **Three-state outputs glitch-free during power-up and power-down**
- **I_{OL}: 48 mA Commercial**
- **Higher speed, lower power version of the Am29827**

GENERAL DESCRIPTION

The Am29827A Bus Buffer provides high performance bus interface buffering for wide address/data paths or buses carrying parity. The device features a 10-bit wide data path and NORed output enables for maximum control flexibility. The Am29827A has non-inverting outputs, and features data inputs with 200 mV minimum input hysteresis to provide improved noise immunity. The

Am29827A is produced with AMD's proprietary IMOX™ bipolar process, and features typical propagation delays of 5 ns.

Each member of the Am29800A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both inputs and outputs.

BLOCK DIAGRAM

07139-001A

IMOX is a trademark of Advanced Micro Devices Inc.

CONNECTION DIAGRAM
(Top View)

DIP

```
        ___
        OE₁ ⌷ 1●    24 ⌷ Vcc
        D₀  ⌷ 2     23 ⌷ Y₀
        D₁  ⌷ 3     22 ⌷ Y₁
        D₂  ⌷ 4     21 ⌷ Y₂
        D₃  ⌷ 5     20 ⌷ Y₃
        D₄  ⌷ 6     19 ⌷ Y₄
        D₅  ⌷ 7     18 ⌷ Y₅
        D₆  ⌷ 8     17 ⌷ Y₆
        D₇  ⌷ 9     16 ⌷ Y₇
        D₈  ⌷ 10    15 ⌷ Y₈
        D₉  ⌷ 11    14 ⌷ Y₉
                          ___
        GND ⌷ 12    13 ⌷ OE₂
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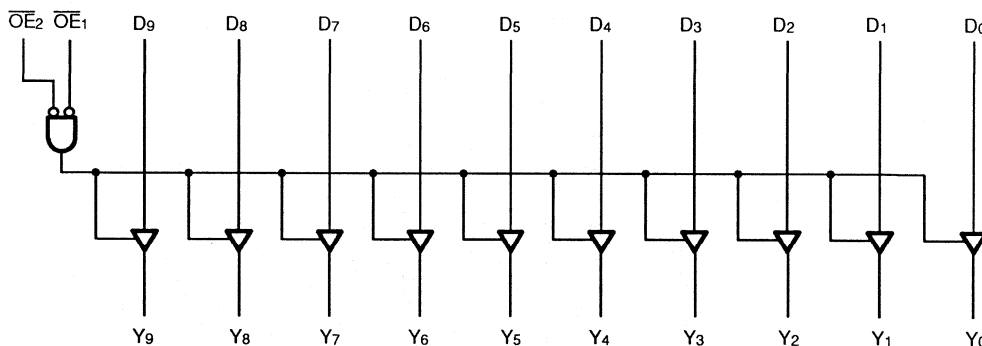
07139-002A

LOGIC SYMBOL

D_i ——10—— ▷ ——10—— Y_i

$\overline{OE}_1$ ——

$\overline{OE}_2$ ——

07139-003A

FUNCTION TABLE

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

Am29827A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

AM29827A   **P**   **C**

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29827A
10-Bit Buffer (Noninverting)

Valid Combinations	
AM29827A	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{OE}_i$
Output Enables (Input, Active LOW)

When both Output Enables are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are Hi-Z.

D_i
Data Inputs (Input)

D_i are the 10-bit data inputs.

Y_i
Data Outputs (Output)

Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Temperature with Power Applied	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−1.5 V to +6.0 V
Output Current, into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T$_A$)	0 to +70°C
Supply Voltage (V$_{CC}$)	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V$_{OH}$	Output HIGH Voltage	V$_{CC}$ = 4.5 V	I$_{OH}$ = −15 mA	2.4		V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −24 mA	2.0		
V$_{OL}$	Output LOW Voltage	V$_{CC}$ = 4.5 V	I$_{OL}$ = 48 mA		0.5	V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$				
V$_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V$_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	V
V$_I$	Input Clamp Voltage	V$_{CC}$ = 4.5 V, I$_{IN}$ = −18 mA			−1.2	V
V$_{HYST}$	Input Hysteresis			200		mV
I$_{IL}$	Input LOW Current	V$_{CC}$ = 5.5 V, V$_{IN}$ = 0.4 V			−0.5	mA
I$_{IH}$	Input HIGH Current	V$_{CC}$ = 5.5 V, V$_{IN}$ = 2.7 V			50	μA
I$_I$	Input HIGH Current	V$_{CC}$ = 5.5 V, V$_{IN}$ = 5.5 V			100	μA
I$_{OZH}$	Output Off-State Current	V$_{CC}$ = 5.5 V, V$_O$ = 2.7 V			50	μA
I$_{OZL}$	(High Impedance)	V$_{CC}$ = 5.5 V, V$_O$ = 0.4 V			−50	μA
I$_{SC}$	Output Short-Circuit Current	V$_{CC}$ = 5.5 V, V$_O$ = 0 V (Note 2)		−75	−250	mA
I$_{OFF}$	Bus Leakage Current	V$_{CC}$ = 0 V, V$_{OUT}$ = 2.9 V			100	μA
I$_{CC}$	Supply Current	V$_{CC}$ = 5.5 V	Outputs LOW		80	mA
		Outputs	Outputs HIGH		55	
		Unloaded	Outputs Hi-Z		70	

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.

2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t_{PLH}	Data (D_i) to Output (Y_i)			8	ns
t_{PHL}				8	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	$C_L = 50$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$		11	ns
t_{ZL}				12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i			10	ns
t_{LZ}				10	ns

*See test circuit and waveforms (Chapter 2).

Am29833A/Am29853A

Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- **High-speed bidirectional bus transceivers for processor organized devices**
  - T-R delay = 6 ns typical
  - R_i-Parity delay = 9 ns typical
- **Error flag with open-collector output**
- **Generates odd parity for all-zero protection**

- **200 mV minimum input hysteresis (Commercial) on input data ports**
- **High drive capability:**
  - 48 mA Commercial I_{OL}
- **Higher speed, lower power versions of the Am29833 & Am29853**

GENERAL DESCRIPTION

The Am29833A and Am29853A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an $\overline{ERR}$ flag showing the result of the parity test.

In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables

are disabled in the Am29853A and Am29833A, the parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

Each of these devices is produced with AMD's proprietary IMOX™ bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability.

SIMPLIFIED BLOCK DIAGRAM

07140-001A

IMOX is a trademark of Advanced Micro Devices, Inc.
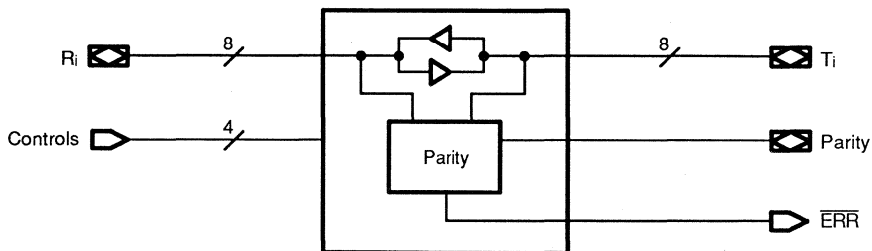
BLOCK DIAGRAMS
Am29833A
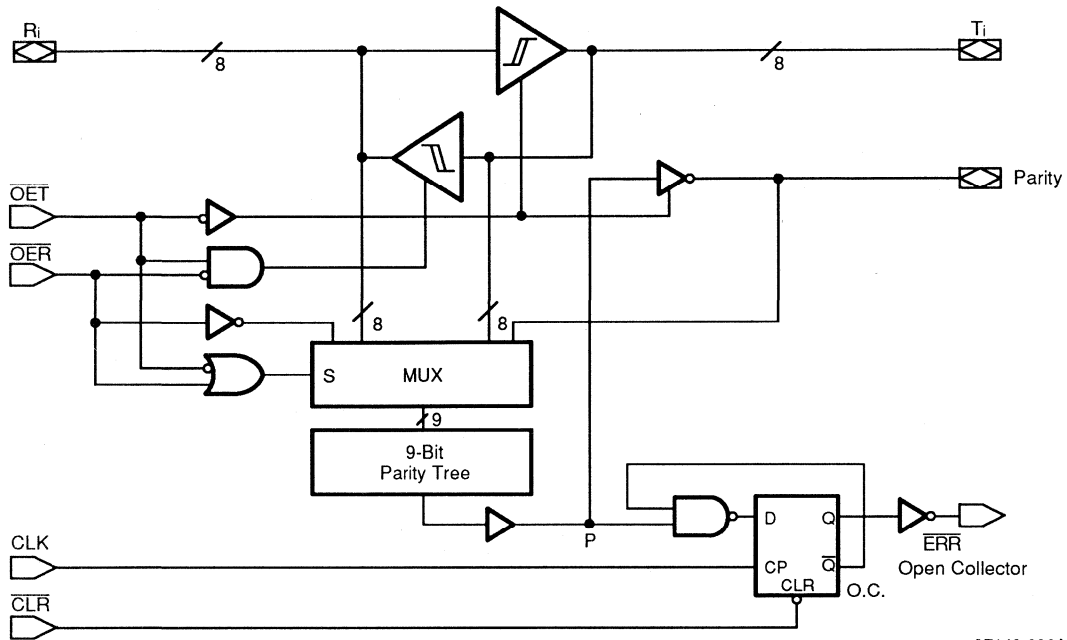
07140-002A

Am29853A

07140-003A

Am29833A

DIP

```
        _____
OER [ 1 •     24 ] Vcc
 R0 [ 2       23 ] T0
 R1 [ 3       22 ] T1
 R2 [ 4       21 ] T2
 R3 [ 5       20 ] T3
 R4 [ 6       19 ] T4
 R5 [ 7       18 ] T5
 R6 [ 8       17 ] T6
 R7 [ 9       16 ] T7
ERR [ 10      15 ] Parity
CLR [ 11      14 ] OET
GND [ 12      13 ] CLK
```

07140-004A

Am29853A

DIP

```
        _____
OER [ 1 •     24 ] Vcc
 R0 [ 2       23 ] T0
 R1 [ 3       22 ] T1
 R2 [ 4       21 ] T2
 R3 [ 5       20 ] T3
 R4 [ 6       19 ] T4
 R5 [ 7       18 ] T5
 R6 [ 8       17 ] T6
 R7 [ 9       16 ] T7
ERR [ 10      15 ] Parity
CLR [ 11      14 ] OET
GND [ 12      13 ] EN
```
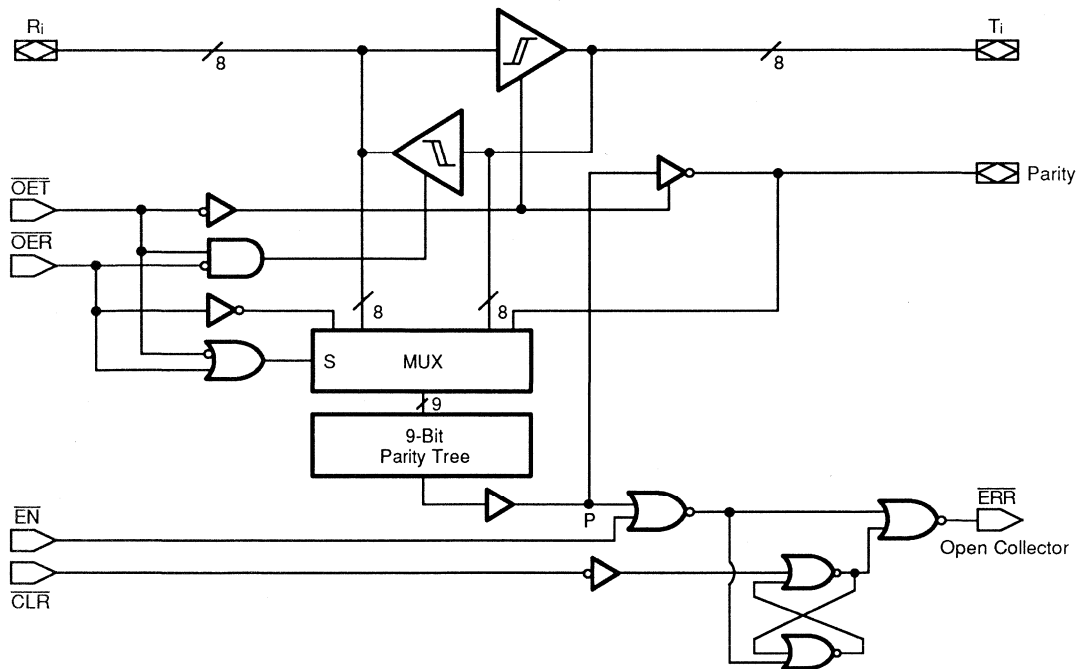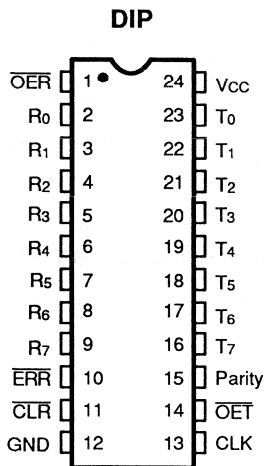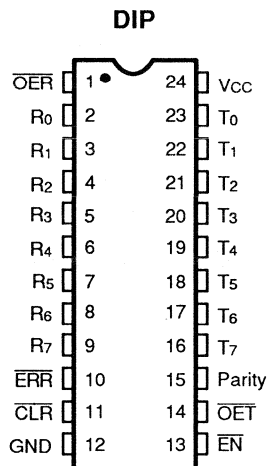
07140-005A

FUNCTION TABLE
Am29833A (Register Option)

$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	Parity logic defaults to transmit mode. Forced-error checking.
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

FUNCTION TABLE
Am29853A (Latch Option)

			Inputs							Outputs			
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's of (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode:
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	transmits data from
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	R port to T port,
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	generating parity. Receive path is disabled.
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode:
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	transmits data from
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	T port to R port with
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode:
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	transmits data from
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	T port to R port,
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and
H	H	L	H	X	X	X	X	Z	Z	Z	H	receiving paths are
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	disabled. Parity logic
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	defaults to transmit mode.
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	checking.
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLES
Error Flag Output
Am29833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	
H	↑	X	L	L	Sample (1's Capture)
H	↑	L	X	L	
L	X	X	X	H	Clear

Note:

$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

Am29853A

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	
L	H	X	L	L	Sample (1's Capture)
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note:

$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

AM29833A
AM29853A
    P   **C**

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29833A
Parity Transceiver, Register Option

Am29853A
Parity Transceiver, Latch Option

Valid Combinations	
AM29833A	PC
AM29853A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION
Am29833A/Am29853A
$\overline{\text{OER}}$
Output Enable Receive (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OET}}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{\text{OET}}$
Output Enable Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OER}}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i
Receive Port (Input/Output, Three-State)

R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output, Three-State)

T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity
Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29833A Only
$\overline{\text{ERR}}$
Error Flag (Output, Open Collector)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the register is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, the Error Flag Register is cleared ($\overline{\text{ERR}}$ goes HIGH).

CLK
Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

Am29853A Only
$\overline{\text{ERR}}$
Error Flag (Output, Open Collector)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the latch is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, and $\overline{\text{EN}}$ is HIGH, the Error Flag latch is cleared ($\overline{\text{ERR}}$ goes HIGH).

$\overline{\text{EN}}$
Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −65°C to +150°C

Ambient Temperature with
Power Applied −55 to +125°C

Supply Voltage to Ground
Potential Continuous −0.5 V to +7.0 V

DC Voltage Applied to Outputs For
High Output State −0.5 V to +5.5 V

DC Input Voltage −1.5 V to +6.0 V

DC Output Current, Into Outputs 100 mA

DC Input Current −30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Ambient Temperature (T_A) 0 to +70°C
Supply Voltage (V_{CC}) +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V,		I_{OH} = −15 mA	2.4		V
	Except ($\overline{ERR}$)	V_{IN} = V_{IH} or V_{IL}		I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V,	$\overline{ERR}$	I_{OL} = 48 mA		0.5	V
		V_{IN} = V_{IH} or V_{IL}	All Other Outputs	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i				200		mV
I_{ZL}	I/O Port LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V				−550	μA
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V				−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				100	μA
I_{ZH}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				100	μA
I_{ZI}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				150	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_O = 2.9 V				100	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5 V Outputs Loaded	Outputs LOW			180	mA
			Outputs HIGH			155	
			Outputs Hi-Z			170	

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.

2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions*	Min.	Max.	Unit
t_{PLH}	Propagation Delay to R_i to T_i,				10	ns
t_{PHL}	T_i to R_i				10	ns
t_{PLH}	Propagation Delay R_i to Parity				15	ns
t_{PHL}					15	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity			12		ns
t_{ZL}					12	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i and Parity			12		ns
t_{LZ}					12	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)		$C_L = 50$ pF $R_1 = 500\ \Omega$ $R_2 = 500\ \Omega$	12		ns
t_H	T_i, Parity to CLK Hold Time (Note 1)			0		ns
t_{REC}	Clear ($\overline{CLR}$ ⌐) to CLK Setup Time (Note 2)			15		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		7		ns
t_{PWL}		LOW		7		ns
t_{PWL}	Clear Pulse Width	LOW		7		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				12	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				16	ns
t_{PLH}	Propagation Delay T_i, Parity to $\overline{ERR}$ (PASS Mode Only) Am29853A				22	ns
t_{PHL}					18	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity				15	ns
t_{PHL}					15	ns

*See test circuit and waveforms (Chapter 2).

Notes:

1. For Am29853A, replace CLK with $\overline{EN}$.
2. Not applicable to Am29853A.

Am29841/Am29843

High Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- **High speed parallel latches**
  - Noninverting transparent t_{PD} = 5.25 ns typ
  - Inverting transparent t_{PD} = 6.0 ns typ
- **Buffered common latch enable, clear and preset input**
- **Three-state outputs glitch free during power-up and down**
- **Outputs have Schottky clamp to ground**
- **48 mA Commercial I_{OL}**

- **Low input/output capacitance**
  - 6 pF inputs (typical)
  - 8 pF outputs (typical)
- **I_{OH} specified 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **Fully TTL compatible inputs and outputs**
- **IMOX™ high performance IMplanted OXide isolated process**

GENERAL DESCRIPTION

The Am29841/843 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 is a buffered, 10-bit wide version of the popular '373 function. The Am29843 is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems.

All of the Am29800 high performance interface family is designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAMS
Am29841
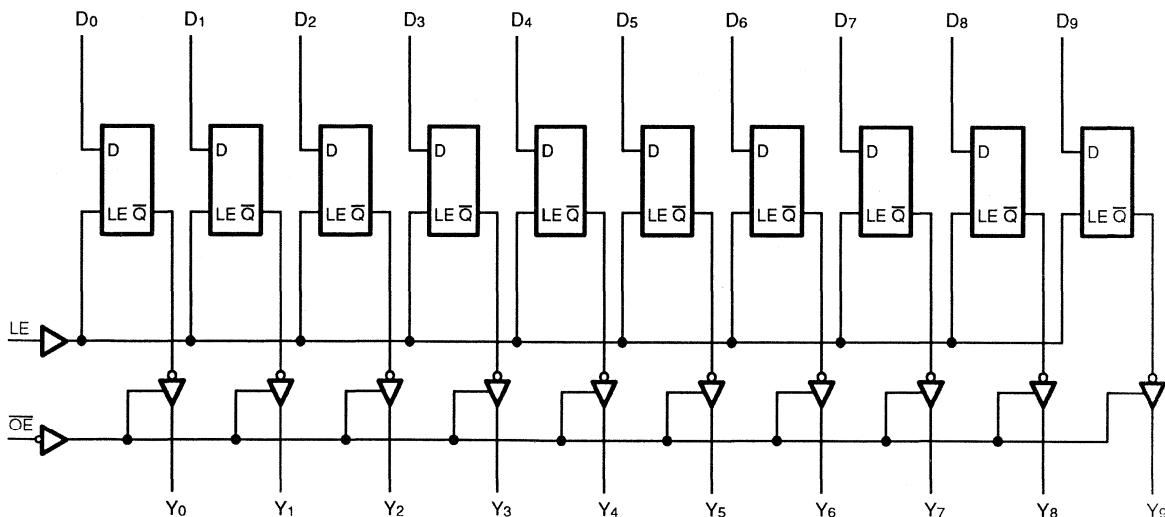
01972-001A

BLOCK DIAGRAMS (Continued)
Am29843

01972-002A

Am29841/Am29843

Am29841

DIP

01972-003A

Am29843

DIP
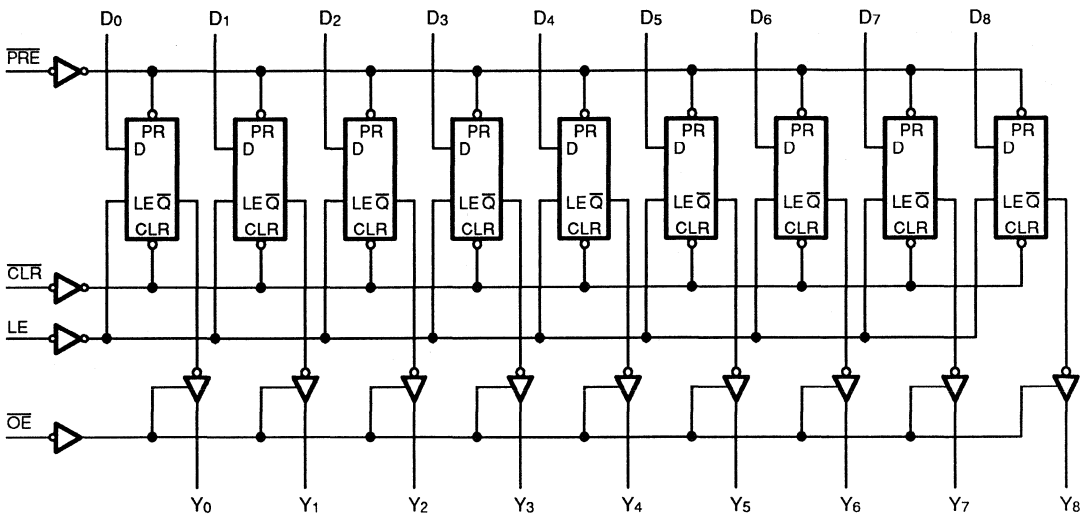
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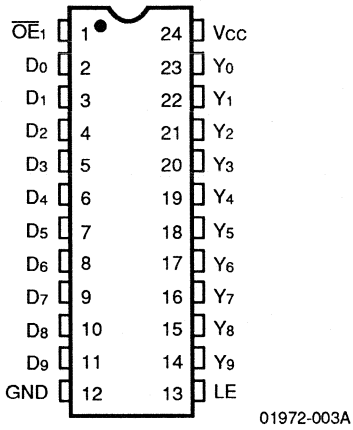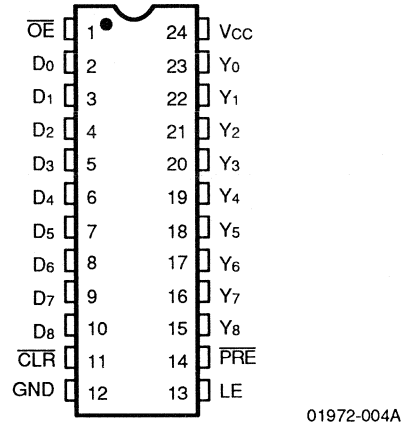
LOGIC SYMBOLS

Am29841
10-Bit Latch
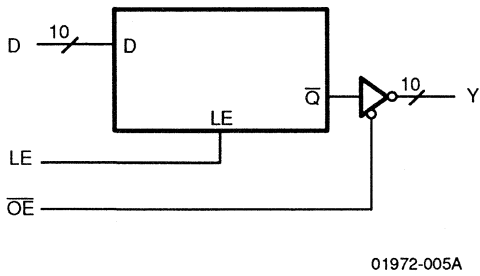
01972-005A

Am29843
9-Bit Latch
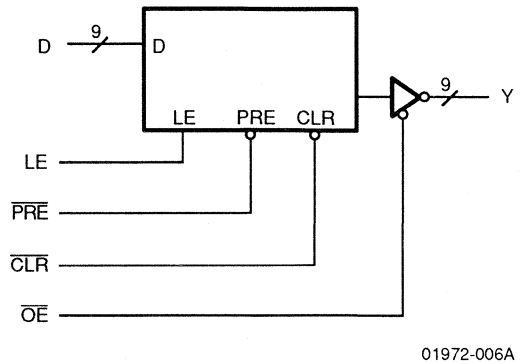
01972-006A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**

AM29841
AM29843　　　　　　　　**P**　　**C**

e. **OPTIONAL PROCESSING**
Blank = Standard processing

d. **TEMPERATURE RANGE**
C = Commercial (0 to +70°C)

c. **PACKAGE TYPE**
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. **SPEED OPTION**
Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**
Am29841
10-Bit Noninverting Latch

Am29843
9-Bit Noninverting Latch
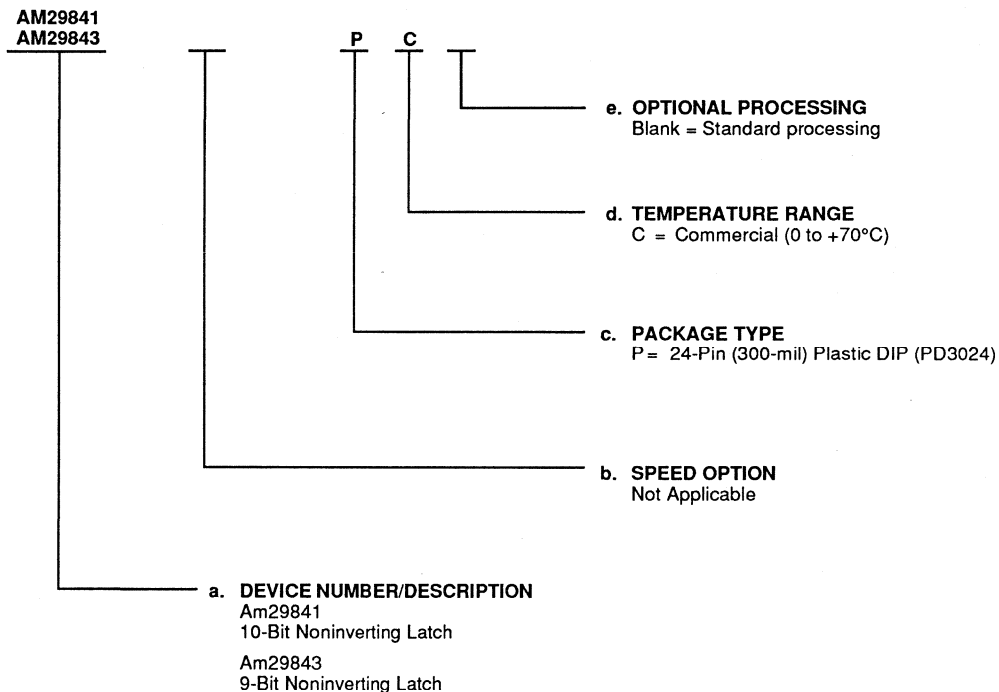
Valid Combinations	
AM29841	PC
AM29843	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{CLR}$

When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

D_i

The latch data inputs.

LE

The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i

The 3-state latch outputs.

$\overline{OE}$

The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

$\overline{PRE}$

Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

Am29841

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi–Z
H	H	L	H	Z	Hi–Z
H	H	H	L	Z	Hi–Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29843

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi–Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	5.0 V ± 10% 4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			1.0	mA
I_{OZ}	Output Off-State (Hi-Z) Output Current	V_{CC} = 5.5 V	V_O = 0.4 V		−50	μA
			V_O = 2.4 V		50	
I_{SC}	Output Short Circuit Current (Note 1)	V_{CC} = 5.5 V		−75	−250	mA
I_{CC}	Supply Current	V_{CC} = 5.5 V Outputs Open	Over Temperature Range		120	mA
			+70°C		110	

Note:

1. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Typ.	Max.	Unit
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF	3.5	5.7	8	ns
t_{PHL}				3.5	6.2	8	ns
t_{PLH}			C_L = 300 pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50 pF	2.0	−0.2		ns
t_H	Data to LE Hold Time			2.5	0.7		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50 pF		8	10.5	ns
t_{PHL}					7.5	10	ns
t_{PLH}			C_L = 300 pF			15	ns
t_{PHL}						15	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50 pF		6.5	9	ns
t_S	Preset Recovery ($\overline{PRE}$ ⌐) Time				7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i				15	18	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time				7.8	12	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50 pF	4	2.5		ns
t_{PWL}	Preset Pulse Width	LOW		5			ns
t_{PWL}	Clear Pulse Width	LOW		6			ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		C_L = 300 pF			17	ns
t_{ZL}						21	ns
t_{ZH}			C_L = 50 pF		7.3	12	ns
t_{ZL}					9.7	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i		C_L = 50 pF		10.4	14	ns
t_{LZ}					4.7	11	ns
t_{HZ}			C_L = 5 pF (Note 2)		3.4	8	ns
t_{LZ}					3.8	8	ns

Notes:

1. See test circuit and waveforms (Chapter 2).

2. Not tested.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Max.	Unit
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		$C_L = 50\ pF$	3.5	9.5	ns
t_{PHL}				3.5	9.5	ns
t_{PLH}			$C_L = 300\ pF$		12.5	ns
t_{PHL}					13	ns
t_S	Data to LE Setup Time		$C_L = 50\ pF$	2.5		ns
t_H	Data to LE Hold Time			2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i		$C_L = 50\ pF$		12	ns
t_{PHL}					12	ns
t_{PLH}			$C_L = 300\ pF$		16	ns
t_{PHL}					16	ns
t_{PLH}	Propagation Delay, Preset to Y_i		$C_L = 50\ pF$		12	ns
t_S	Preset Recovery ($\overline{PRE}$ ⌐) Time				14	ns
t_{PHL}	Propagation Delay, Clear to Y_i				21	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time				14	ns
t_{PWH}	LE Pulse Width	HIGH	$C_L = 50\ pF$	6		ns
t_{PWL}	Preset Pulse Width	LOW		8		ns
t_{PWL}	Clear Pulse Width	LOW		8		ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i		$C_L = 300\ pF$		20	ns
t_{ZL}					23	ns
t_{ZH}			$C_L = 50\ pF$		14	ns
t_{ZL}					14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i		$C_L = 50\ pF$		15	ns
t_{LZ}					12	ns
t_{HZ}			$C_L = 5\ pF$		9	ns
t_{LZ}					9	ns

Note:

1. See test circuit and waveforms (Chapter 2).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS
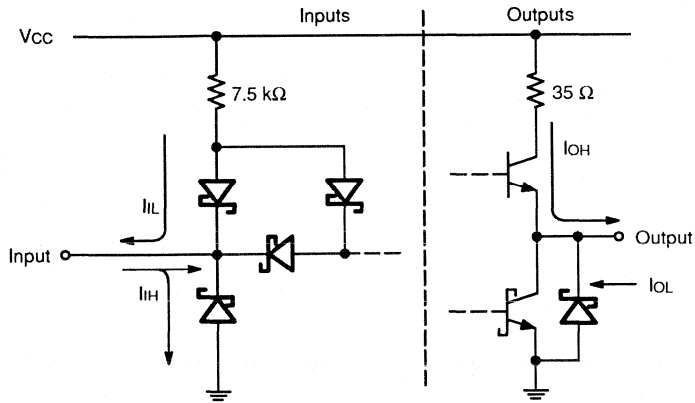
01972-007A

Am29861A

High-Performance Bus Transceiver

DISTINCTIVE CHARACTERISTICS

- High-speed symmetrical bidirectional transceiver
  - t_{PD} = 5 ns typical
- 200–mV minimum input hysteresis on input data ports

- Three-state outputs glitch-free during power-up and down
- I_{OL}: 48 mA commercial
- Higher speed, lower power version of the Am29861

GENERAL DESCRIPTION

The Am29861A Bus Transceiver provides high-performance bus interface buffering for wide address/data paths or buses carrying parity. The device is a 10-bit bidirectional transceiver. The device features data inputs with 200–mV minimum input hysteresis to provide improved noise immunity. The Am29861A is

produced with AMD's proprietary IMOX bipolar process, and features typical propagation delays of 5 ns.

Each member of the Am29800A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both the inputs and outputs.

BLOCK DIAGRAM

07142-001A

CONNECTION DIAGRAM
Top View

DIP

$\overline{OER}$	1	24	V_{CC}
R_0	2	23	T_0
R_1	3	22	T_1
R_2	4	21	T_2
R_3	5	20	T_3
R_4	6	19	T_4
R_5	7	18	T_5
R_6	8	17	T_6
R_7	9	16	T_7
R_8	10	15	T_8
R_9	11	14	T_9
GND	12	13	$\overline{OET}$
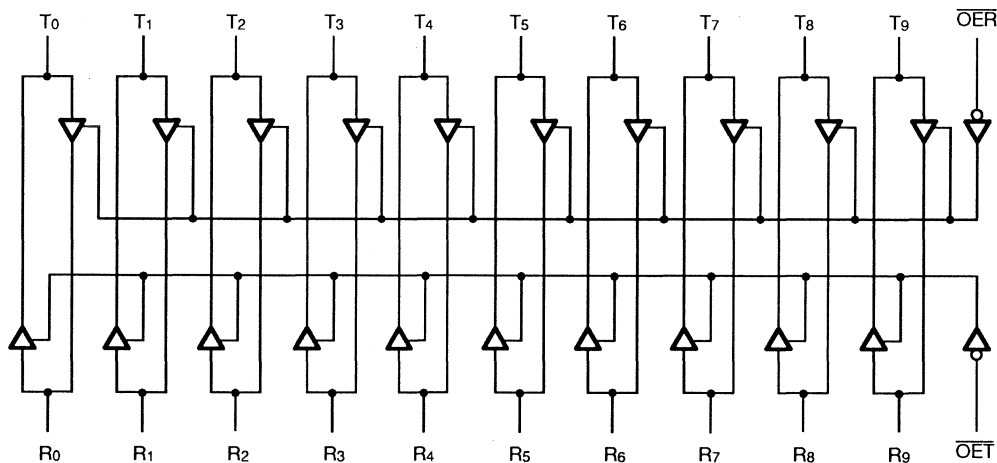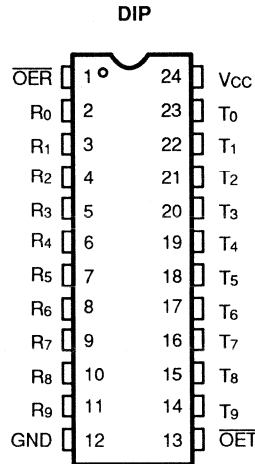
07142-002A

LOGIC SYMBOLS

$\overline{OET}$

R_i — 10 —

10 — T_i

$\overline{OER}$

07142-003A

FUNCTION TABLE

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi–Z

H = HIGH L = LOW
Z = High Impedance X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

AM29861A   **P**   **C**

e. OPTIONAL PROCESSING
Blank = Standard processing
    B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29861A
10-Bit Transceiver
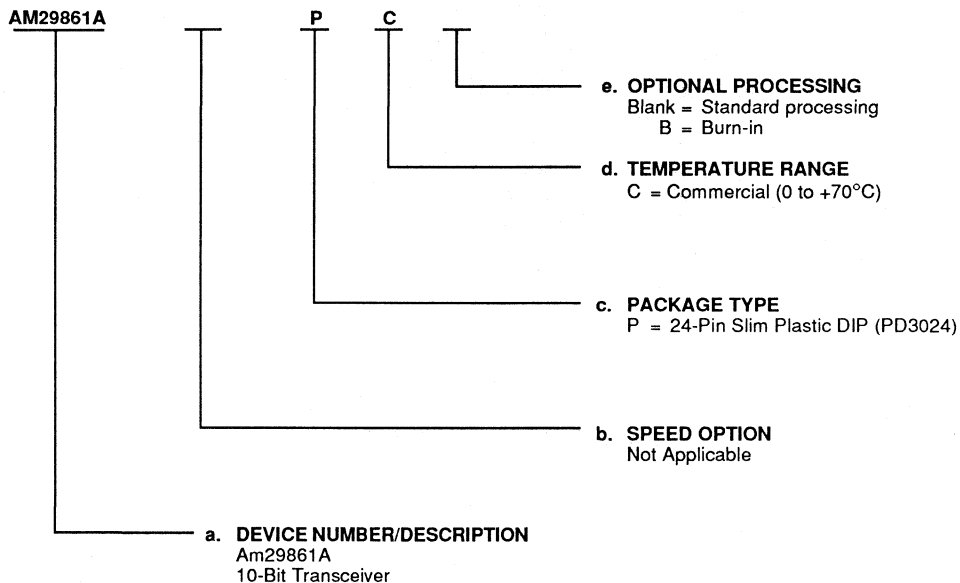
Valid Combinations	
AM29861A	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION
Am29861A

$\overline{OER}$
Output Enable-Receive (Input, Active LOW)

When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$
Output Enable–Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are outputs).

R_i
Receive Port (Input/Output)

R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output)

T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Output For High Output State	−0.5 V to +5.5 V
DC Input Voltage	−1.5 V to +6.0 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Suppy Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
V_{HYST}	Input Hysteresis			200		mV
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	µA
I_{ZL}	I/O Port LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−550	µA
I_{ZH}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			100	µA
I_{ZI}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			150	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	µA
I_{CC}	Supply Current	V_{CC} = 5.5 V Outputs Unloaded	Outputs LOW		140	mA
			Outputs HIGH		115	
			Outputs Hi–Z		130	

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.

2. Not more than one output shorted at a time. Duration of short-circuit test should not exceed one second

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter Description	Parameter Test Conditions*	Min	Max	Unit
t_{PLH}	Propagation Delay from			8	ns
t_{PHL}	R_i to T_i or T_i to R_i			8	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to	$C_L = 50$ pF		11	ns
t_{ZL}	T_i or $\overline{OER}$ to R_i	$R_1 = 500\ \Omega$		12	ns
t_{HZ}	Output Disable Time OET to	$R_2 = 500\ \Omega$		10	ns
t_{LZ}	T_i or $\overline{OER}$ to R_i			10	ns

* See Test Circuit and Waveforms. (Chapter 2)

Am29863

High Performance Bus Transceiver

DISTINCTIVE CHARACTERISTICS

- High-speed symmetrical bidirectional transceiver
  - Noninverting t_{PD} = 5.0 ns typ
  - Inverting t_{PD} = 4.5 ns typ
- 200 mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and -down
- Outputs have Schottky clamp to ground

- 48 mA commercial I_{OL}
- Low input/output capacitance
- I_{OH} specified 2.0 V and 2.4 V
- 24-pin 0.3" space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted OXide isolated process

GENERAL DESCRIPTION

The Am29863 bus transceiver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The Am29863 is a 9-bit transceiver with NOR-ed output enables for maximum control flexibility. All transceiver data inputs have 200 mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

03369-001A

CONNECTION DIAGRAM
Top View

DIP

$\overline{OER_1}$	1	24	V_{CC}
R_0	2	23	T_0
R_1	3	22	T_1
R_2	4	21	T_2
R_3	5	20	T_3
R_4	6	19	T_4
R_5	7	18	T_5
R_6	8	17	T_6
R_7	9	16	T_7
R_8	10	15	T_8
$\overline{OER_2}$	11	14	$\overline{OET_2}$
GND	12	13	$\overline{OET_1}$
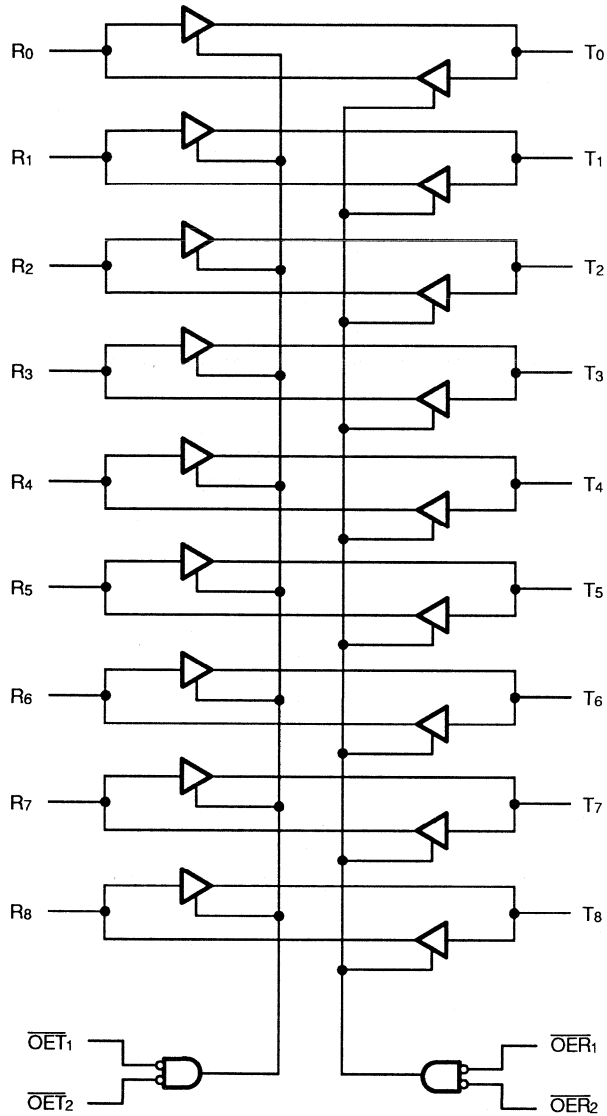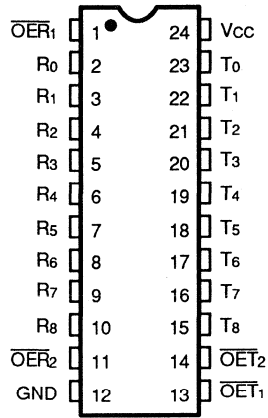
03369-002A

LOGIC SYMBOL
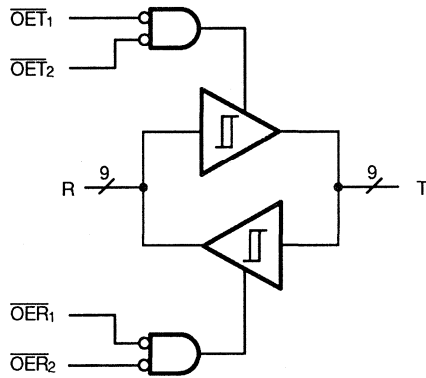
9-Bit Transceiver

03369-003A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Package Type
    d. Temperature Range
    e. Optional Processing

AM29863   P   C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29863
9-Bit Bus Transceiver
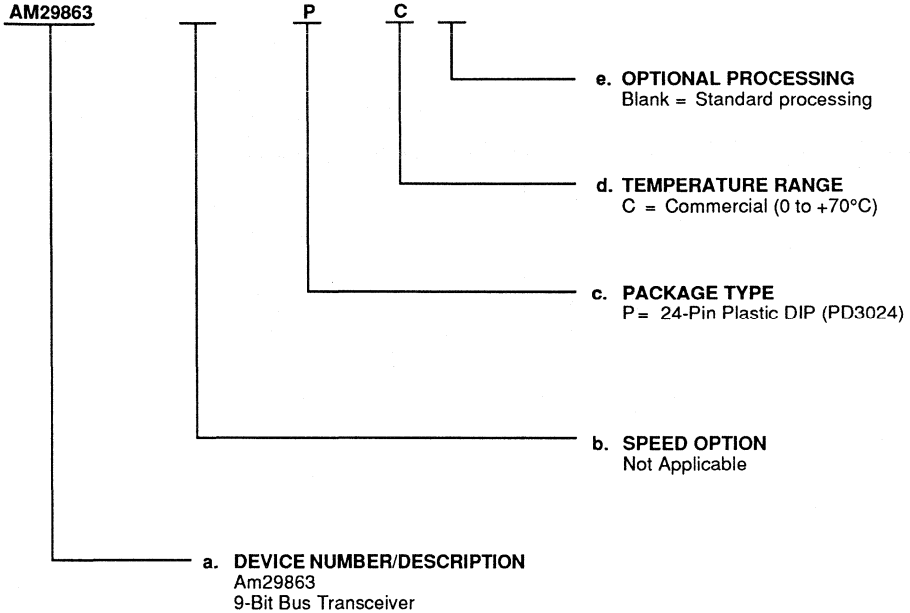
Valid Combinations	
AM29863	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{OER}_i$

When both are LOW in conjunction with any $\overline{OET}_i$ HIGH indicates the RECEIVE mode.

$\overline{OET}_i$

When both are LOW in conjunction with any $\overline{OER}_i$ HIGH indicates the TRANSMIT mode.

R_i

9-bit RECEIVE input/output.

T_i

9-bit TRANSMIT input/output.

FUNCTION TABLE

Inputs						Outputs		
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_i	T_i	R_i	T_i	Function
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H   =   HIGH

L   =   LOW

Z   =   High Impedance

X   =   Don't Care

N/A =   Not Applicable

Am29863

ABSOLUTE MAXIMUM RATINGS

Storage Temperature   −65°C to +150°C

Ambient Temperature with
Power Applied   −55°C to +125°C

Supply Voltage to Ground
Potential Continuous   −0.5 V to +7.0 V

DC Voltage Applied to Output
for High Output State   −0.5 V to +5.5 V

DC Input Voltage   −0.5 V to +5.5 V

DC Output Current, Into Outputs   100 mA

DC Input Current   −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)   0 to +70°C

Supply Voltage (V_{CC})   5.0 V ± 10%
                                           +4.5 V to +5.5 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4		V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −24 mA	2.0		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.5	V
		V_{IN} = V_{IH} or V_{IL}				
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
V_{HYST}	Input Hysteresis	Tested output is connected to AC load test circuit		200		mV
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} 5.5 V			1.0	mA
I_{OZH}	Output Off-State Output Current (Hi-Z)	V_{CC} = 5.5 V, V_O = 2.4 V			50	μA
I_{OZL}	Output Off-State Output Current (Hi-Z)	V_{CC} = 5.5 V, V_O = 0.4 V			−1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V		−75	−250	mA
I_{CC}	Supply Current	V_{CC} = 5.5 V	Over Temperature Range		160	mA
		Outputs Open	+70°C		150	

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i	C_L = 50 pF		4.8	6.0	ns
t_{PHL}				5.2	6.2	ns
t_{PLH}		C_L = 300 pF		8	11	ns
t_{PHL}				11	14	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i and $\overline{OER}$ to R_i	C_L = 50 pF		6.5	12	ns
t_{ZL}				9.5	12	ns
t_{ZH}		C_L = 300 pF		11	17	ns
t_{ZL}				17	21	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i and $\overline{OER}$ to R_i	C_L = 5 pF		3.5	8.0	ns
t_{LZ}				3.5	8.0	ns
t_{HZ}		C_L = 50 pF		11.2	16	ns
t_{LZ}				4.5	9.0	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i	C_L = 50 pF		8	ns
t_{PHL}				8	ns
t_{PLH}		C_L = 300 pF		15	ns
t_{PHL}				15	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 50 pF		15	ns
t_{ZL}				15	ns
t_{ZH}		C_L = 300 pF		20	ns
t_{ZL}				23	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 5 pF		9	ns
t_{LZ}				9	ns
t_{HZ}		C_L = 50 pF		17	ns
t_{LZ}				12	ns

*See Test Circuit and Waveforms (Chapter 2).

CHAPTER 6
Packaging-Physical Dimensions

PD3024
24-Pin 300-mil Plastic SKINNYDIP

07089F-002
BC 4
12/10/90 cd
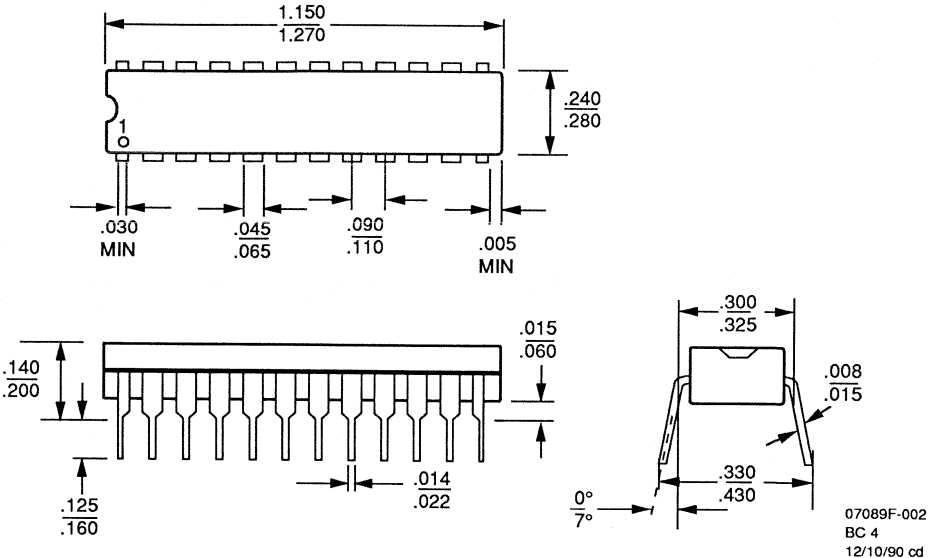
Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

CD3024
24-Pin 300-mil Ceramic SKINNYDIP
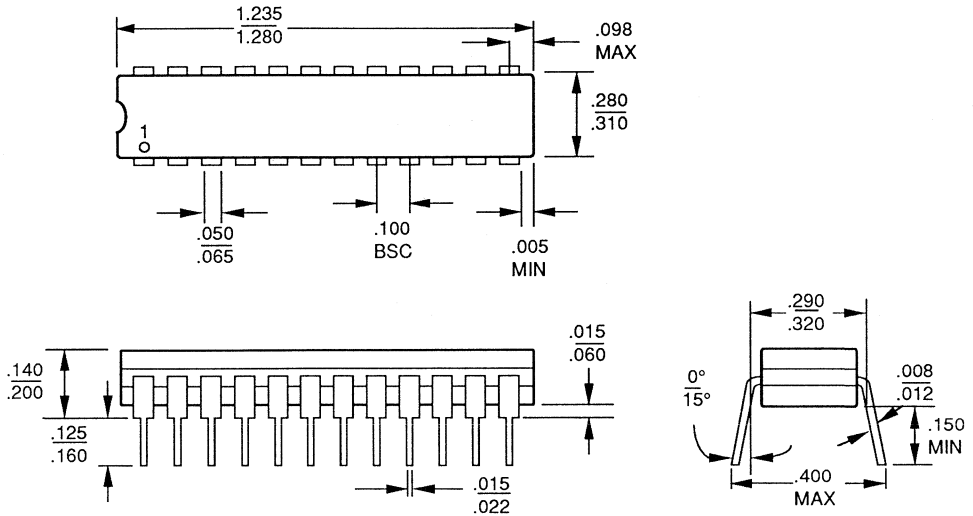
06850C

PL 028
28-Pin Plastic Leaded Chip Carrier
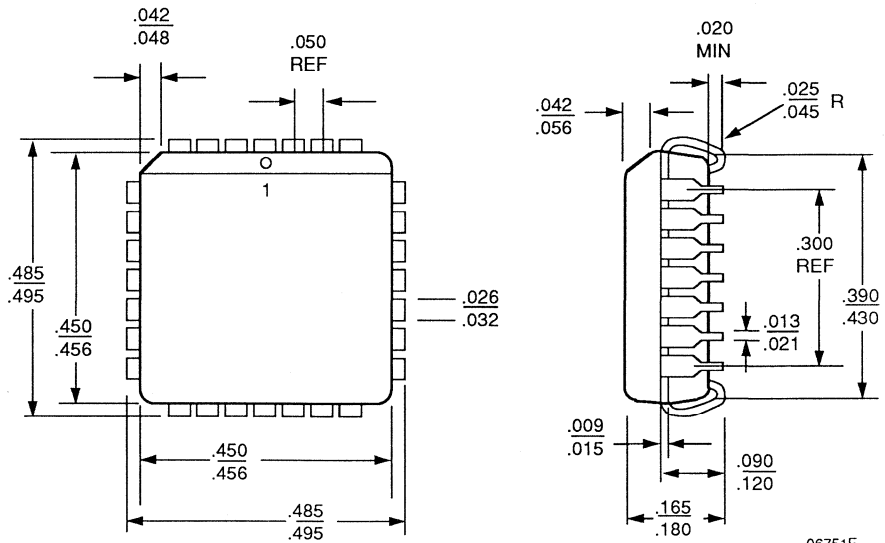
06751E

SO 024
24-Pin Plastic Small Outline Package
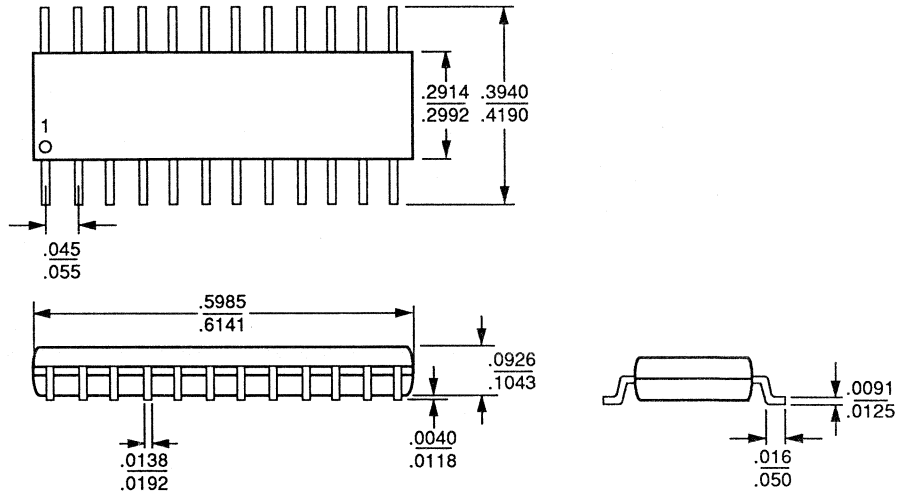
09310B

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- Am29C833A, Am29841A, Am29C843A, Am29C853A, Am29C861A, Am29C863A

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- Am29C982
- Am29C983, Am29C983A
- Am29C985

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■ Am29C833A, Am29C841A, Am29C843A, Am29C853A, Am29C861A, Am29C863A

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■ Am29C982
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